Charging System Safety Device

General Description

The RT9730 is an integrated circuit (IC) designed to replace passive device in charging system with extra protection function. It is optimized to protect low voltage system from up to 28V high voltage input. The IC monitors the input voltage to make sure all parameters are operating in normal range. It also monitors its own temperature and turns off the MOSFET when the chip temperature exceeds 140°C. When the input voltage exceeds the threshold, the IC turns off the power MOSFET within 1μs to remove the power before any damage occurs. User can monitor the adapter input voltage from the CHRIN pin, which has 50mA current capability. The gate of the P-MOSFET will be controlled by the external charging controller from GATDRV pin if all parameters are operating in normal range.

The RT9730 is available in a WDFN-8L 2x2 tiny package to achieve best solution for PCB space and total BOM cost saving considerations.

Ordering Information

RT9730□□

Package Type
QW : WDFN-8L 2x2 (W-Type)
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

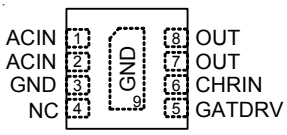
- **No External Blocking Diode Requiring**
- **Over Voltage Turn Off Time of Less Than 1μs**
- **High Accuracy Protection Thresholds**
- **Over Temperature Protection**
- **High Immunity of False Triggering Under Transients**
- **Thermal Enhanced 8-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Cellular Phones
- Digital Cameras
- PDAs and Smart Phones
- Portable Instruments

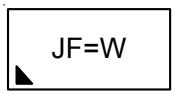
Pin Configurations

(TOP VIEW)



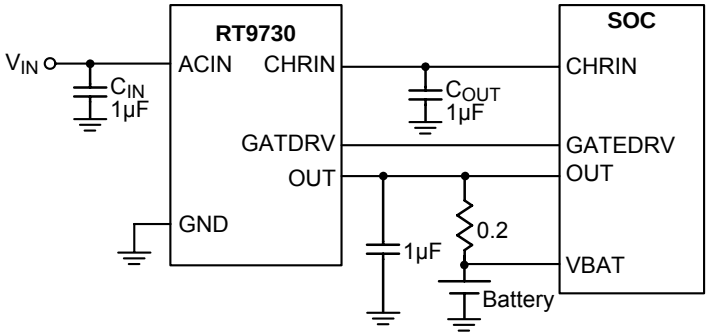
WDFN-8L 2x2

Marking Information



JF= : Product Code
W : Date Code

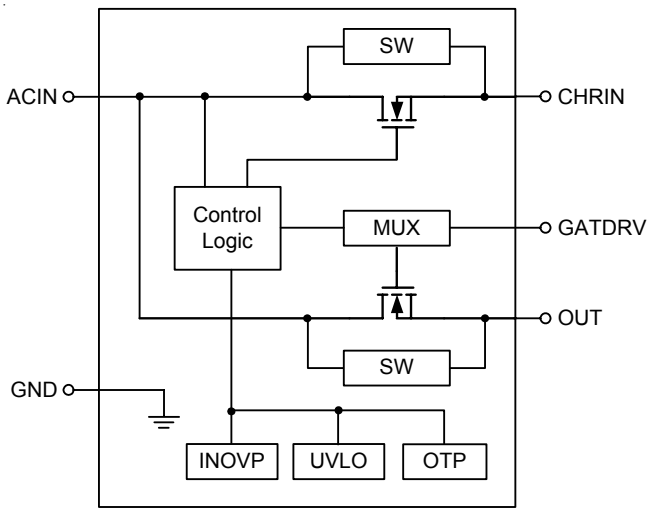
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	ACIN	Input Power Source Pin. It can withstand up to 30V input.
3, 9 (Exposed pad)	GND	Analog Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation..
4	NC	No Internal Connection.
5	GATDRV	External control pin for controlling the P-MOSFET by charging controller.
6	CHRIN	Voltage is equal to VIN as VIN in power good range and providing ≅25mA for system at most.
7, 8	OUT	Connect to OUT resistor and OUT pin of charging controller.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 30V
- Output (as V_{IN} > V_{OUT}, normal mode) ---------- –0.3V to 7V
- Output (as sleep mode) ---------- –0.3V to 4.5V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8L 2x2 ---------- 0.833W
- Package Thermal Resistance (Note 2)
  WDFN-8L 2x2, θ_{JA} ---------- 120°C/W
  WDFN-8L 2x2, θ_{JC} ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	2.5	2.7	2.9	V
VIN Under Voltage Lockout Hysteresis	ΔV_{UVLO}		--	100	--	mV
VIN Bias Current		When enable	--	200	600	μA
Reverse Leakage	$I_{LEAKAGE}$	As ACIN floating	--	5	10	μA
Operation Voltage			4.3	--	6.5	V
Operation Current			--	--	1	A
Protections						
Input OVP Reference Voltage	V_{INOVP}		6	6.25	6.5	V
Input OVP Hysteresis			--	60	100	mV
Input OVP Propagation Delay			--	--	1	μs
OTP Rising Thershold			--	140	--	°C
OTP Hysteresis			--	20	--	°C
Power MOSFET						
$R_{DS(ON)}$ Between ACIN to OUT	$R_{DS(ON)\_OUT}$	Measure @ 500mA. 4.3V < V_{IN} < 6V	--	--	500	mΩ
$R_{DS(ON)}$ Between ACIN to CHRIN	$R_{DS(ON)\_CHRIN}$	Measure @ 50mA. 4.3V < V_{IN} < 6V	--	--	3	Ω

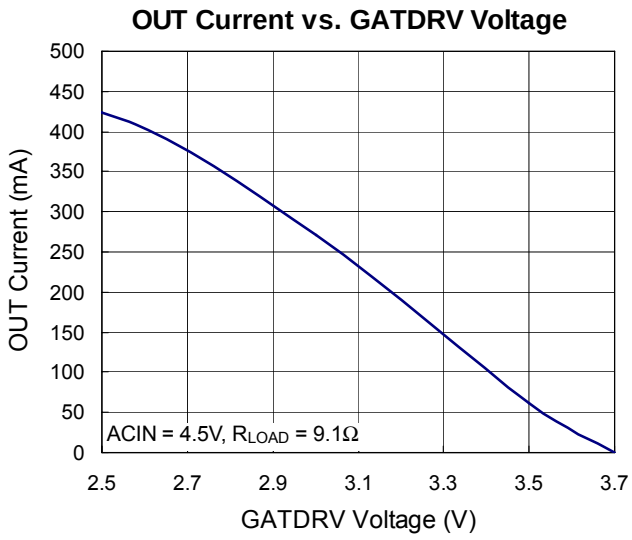
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

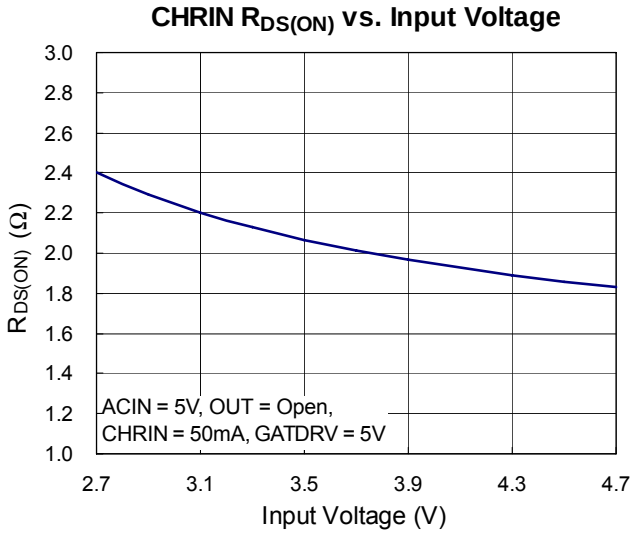
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

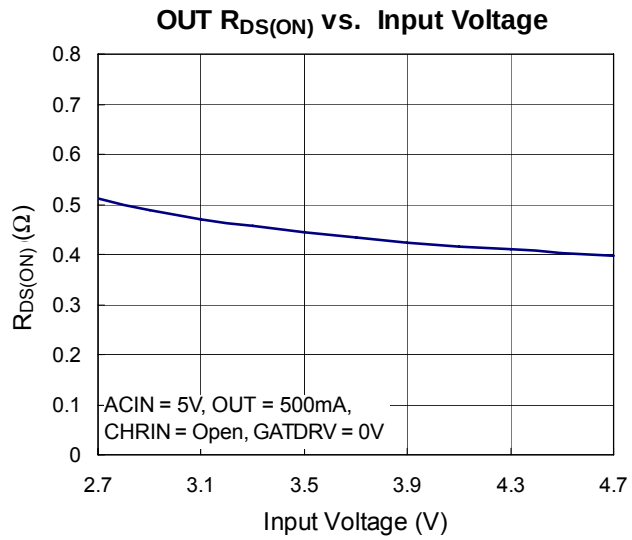
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

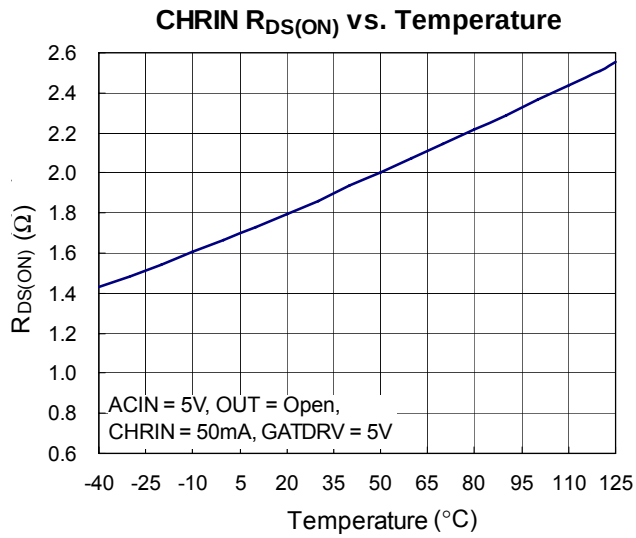
Note 4. The device is not guaranteed to function outside its operating conditions.

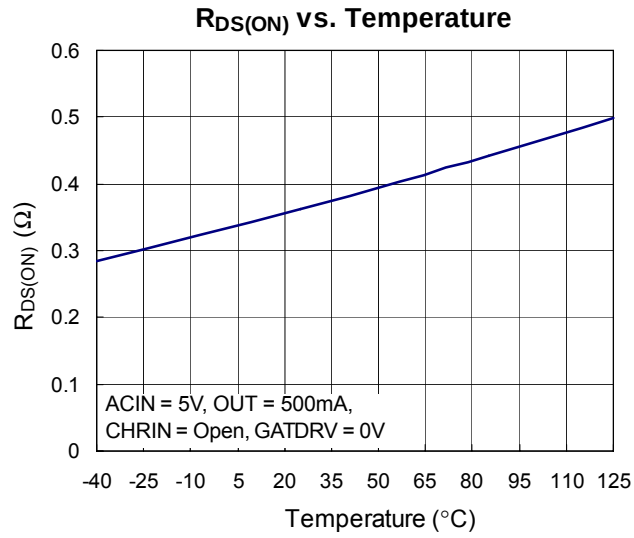
Typical Operating Characteristics

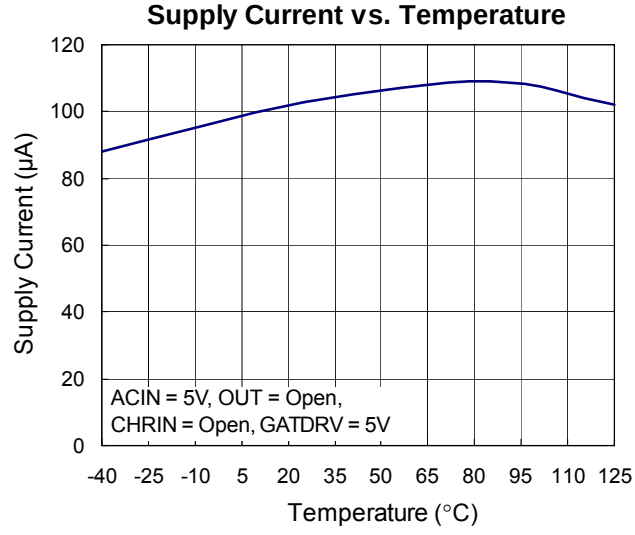




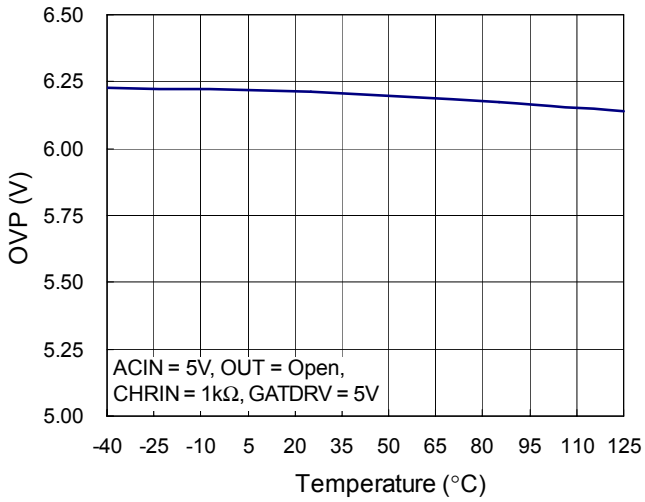




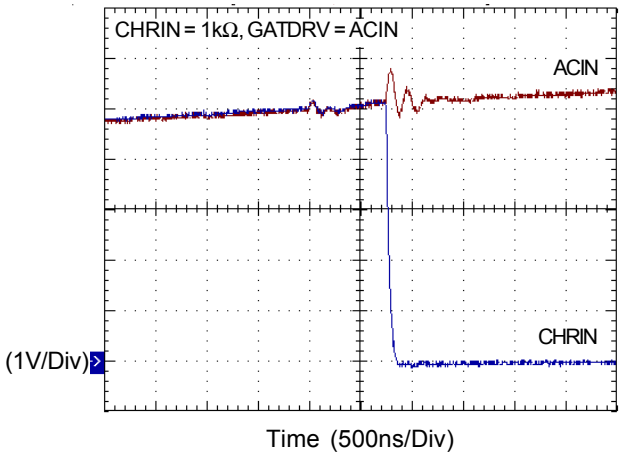




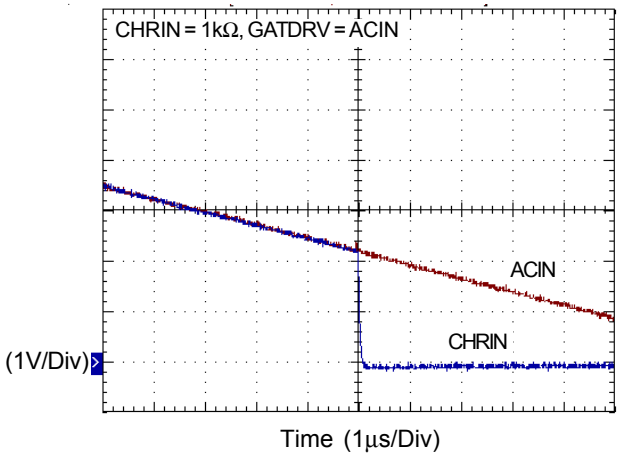
OVP vs. Temperature



Input OVP Propagation Delay



Input OVP Recovery Delay



Application information

Operation State

The operation state is shown in the following Figure 1. At power-off state, the RT9730 will check whether V_{IN} is > UVLO threshold. If V_{IN} is higher than the UVLO threshold, the RT9730 will check whether the junction temperature is over the OTP threshold. If the junction temperature is higher than the OTP threshold, the internal P-MOSFET will be turned off. If the junction temperature is lower than the OTP threshold, the RT9730 will check whether V_{IN} is higher than the OVP threshold or not, if V_{IN} is higher than the OVP threshold, the RT9730 will turn off the internal P-MOSFET immediately within 1μs.

If all of the checks including V_{IN} > UVLO, T_J < OTP and V_{IN} < OVP are ok, the IC will operate normally.

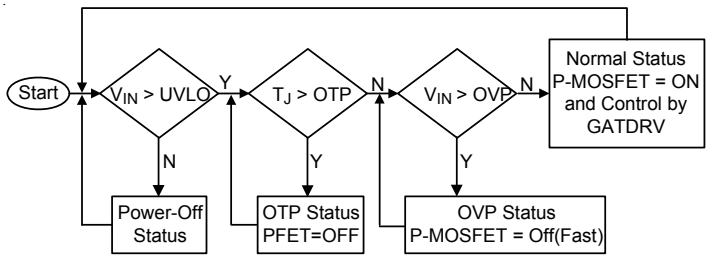


Figure 1. Operation State Diagram for OVP Function

Input Over Voltage Protection (OVP)

The RT9730 monitors the input voltage to prevent abnormally high input voltage from causing output system failures. When the input voltage exceeds the threshold, the RT9730 will turn off the power MOSFET within 1μs to prevent damage to the electronics in the handheld system. The hysteresis for the input OVP threshold is 100mV. When the input voltage returns to normal operation voltage range, the RT9730 re-enables the MOSFET. The RT9730 can with stand an input voltage up to 30V without suffering damage.

Battery Voltage Monitor

The RT9730 monitors the battery voltage by the OUT pin. When the battery voltage exceeds the voltage level of (V_{IN} – 0.2V), the RT9730 will turn off the MOSFET and the battery will not be charged. The RT9730 will recharge the battery when the battery voltage is lower than the voltage level of (V_{IN} – 0.2V).

Internal Over Temperature Protection (OTP)

The RT9730 monitors its own internal temperature to prevent thermal failures. When the internal temperature reaches 140°C with a built-in hysteresis of 20°C, the IC turns off the power MOSFET. The IC does not resume operation until the internal temperature drops below 120°C.

Input Under Voltage Protection (UVLO)

The RT9730 monitors input voltage to prevent abnormally low input voltage from causing output system failures. The RT9730 input under voltage protection threshold is set to 2.7V. When the input voltage is under the threshold, the RT9730 will turn off the power MOSFET within 1μs. When the input voltage returns to normal operation voltage range, the RT9730 re-enables the MOSFET.

System Operation Description

Figure 2 shows the connection of RT9730 in a system diagram. The OUT pin of the SOC will sense the voltage of the 0.2Ω sense resistor and the voltage of the VBAT pin. Then, the GATDRV pin of the SOC can control the MOSFET of the RT9730 accordingly to determine the level of the charge current. The power of the SOC is provided by the CHRIN pin of the RT9730. The RT9730 also provides OVP function to the SOC. Once the input voltage at the ACIN pin is higher than the OVP level, the RT9730 will shutdown to prevent the SOC from damage. If the voltage of the battery connected to the VBAT pin is full, the RT9730 stops charging by turning off the OUT pin. Input and output capacitors of 1μF are recommended to be placed as close to the IC as possible.

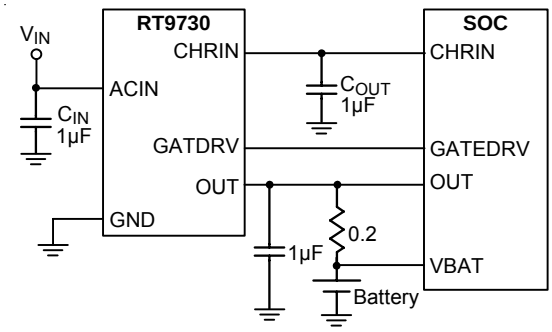


Figure 2. Application Diagram of RT9730 with SOC

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9730, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-8L 2x2 packages, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT9730 package, the derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

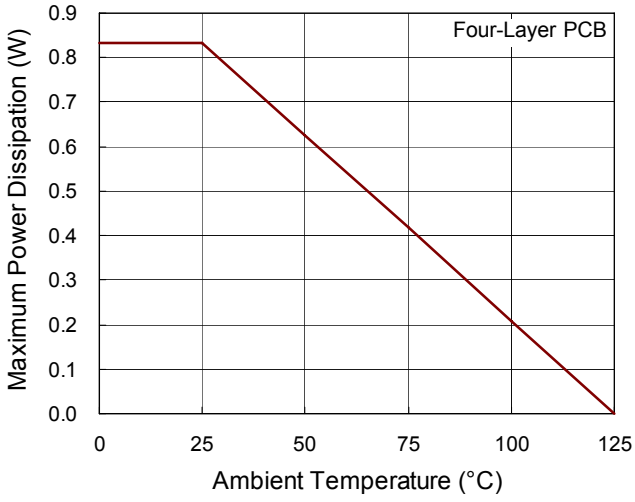


Figure 3. Derating Curves for RT9730 Packages

Layout Consideration

The RT9730 is a protection device. Careful PCB layout is necessary. For best performance, place all peripheral components as close to the IC as possible. A short connection is highly recommended. The following guidelines should be strictly followed when designing a PCB layout for the RT9730.

- The exposed pad, GND, must be soldered to a large ground plane for heat sinking and noise prevention. The through-hole vias located at the exposed pad is connected to the ground plane of internal layer.
- ACIN traces should be wide to minimize inductance and handle the high currents. The trace running from input to chip should be placed carefully and shielded strictly.
- The capacitors must be placed close to the part. The connection between pins and capacitor pads should be copper traces without any through-hole via connection.

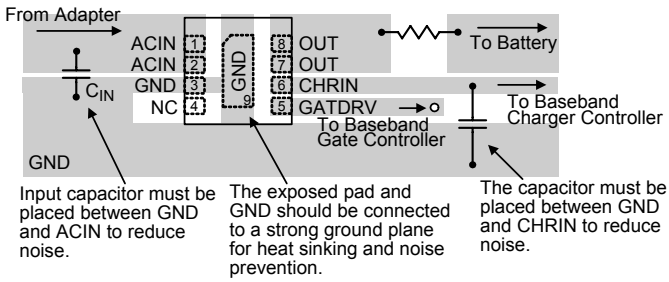
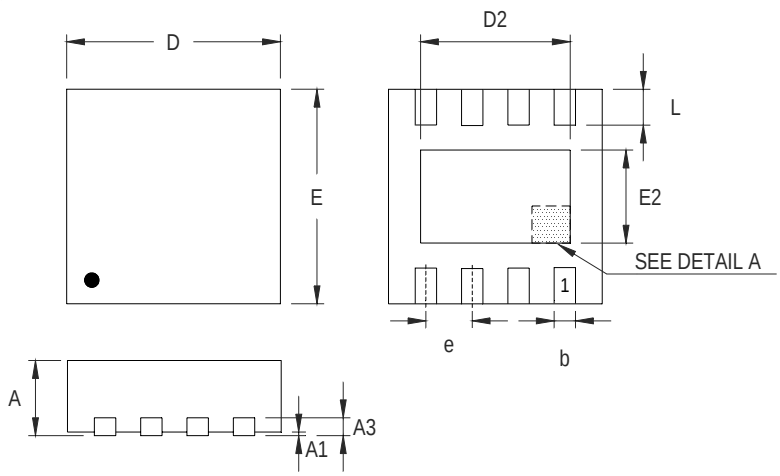
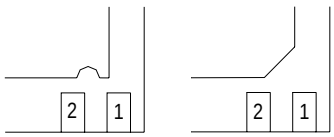


Figure 4. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

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