MOSFET Integrated Smart Photoflash Capacitor Charger with IGBT Driver

General Description

The RT9594A/B are complete photoflash module solutions for digital and film cameras. They are targeted for applications that use 2 to 4 AA batteries or 1 to 2 lithium-ion batteries. The RT9594A/B adopt flyback topology which use constant primary peak current and zero secondary valley current to charge photoflash capacitor quickly and efficiently. The built-in 50V MOSFET allows flexibility in transformer design and simplifies the PCB layout. The RT9594A/B also integrate an IGBT driver for igniting photoflash tube. Only a few external components are required, which greatly reduces the PCB space and cost. The RT9594A/B are available in the WQFN-16L 3x3 package.

Ordering Information

RT9594A/B□□

- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- VDD : 5V (typ.)
- VDD : 3.3V (typ.)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

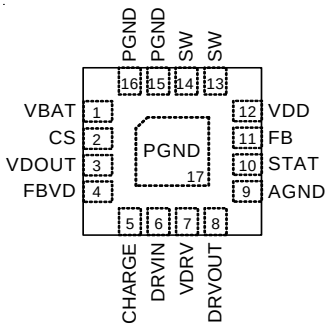
- **50V MOSFET Integrated**
- **1.6V to 9V Battery Input Voltage Range**
- **Two Charge Current Levels Setting**
- **Charges Any Size Photoflash Capacitor**
- **Adjustable Input Current**
- **Adjustable Output Voltage**
- **Charge Complete Indicator**
- **Built-in IGBT Driver for IGBT Application**
- **Constant Peak Current Control**
- **16-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Digital Still Camera
- Film Camera Flash Unit
- Camera Phone Flash

Pin Configurations

(TOP VIEW)



WQFN-16L 3x3

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit

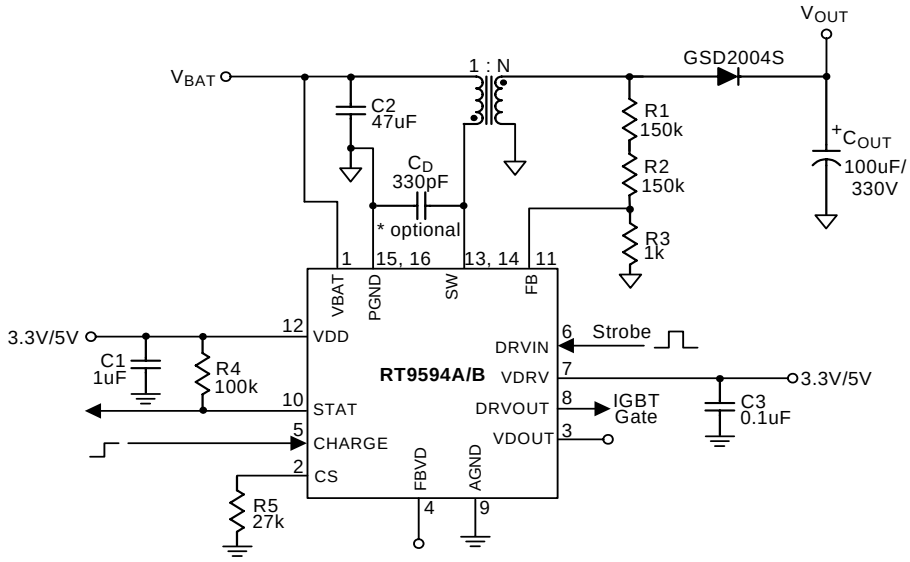


Figure 1. Typical Application Circuit

Note * : If the spike voltage on SW pin is higher than 50V (internal N-MOSFET DC rating) while internal N-MOSFET switches off, place the capacitor (C_D) between SW pin and PGND to reduce the spike voltage.

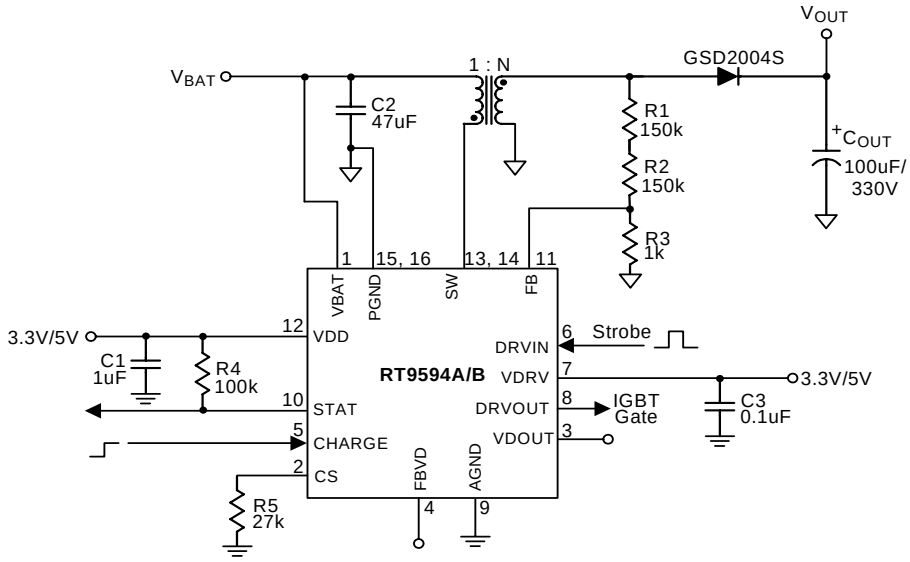
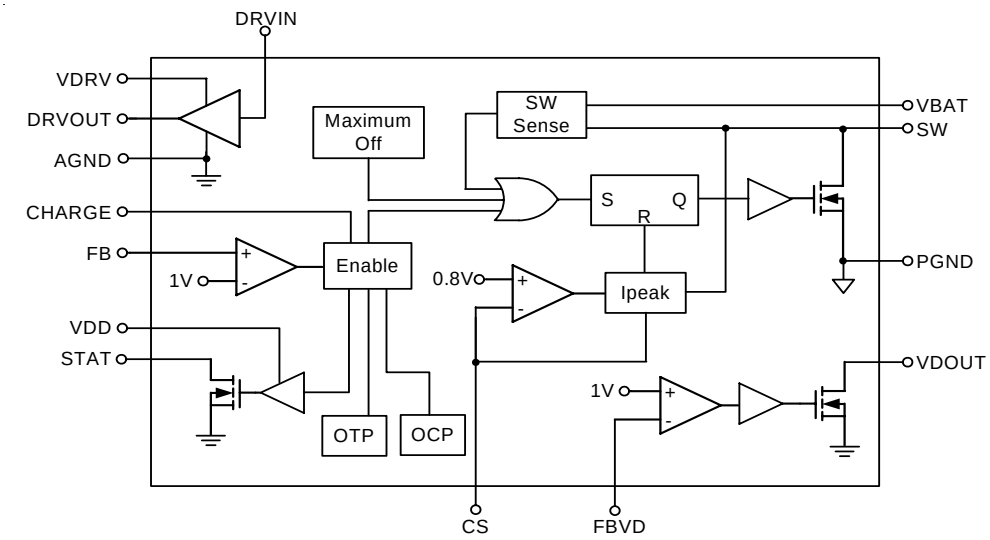


Figure 2. Application Circuit for the Gate Drive Voltage of IGBT Same as VDD Voltage

Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VBAT	Battery Voltage Pin.
2	CS	Input Current Setting Pin.
3	VDOUT	Voltage Detector Output Pin. Open drain output.
4	FBVD	Voltage Detector Feedback Pin.
5	CHARGE	Charge Enable Pin. The charge function is executed when CHARGE pin is set from Low to High. The chip is in Shutdown mode when CHARGE pin is set to Low.
6	DRVIN	IGBT Driver Input Pin.
7	VDRV	IGBT Driver Power Pin.
8	DRVOUT	IGBT Driver Output Pin.
9	AGND	Analog Ground.
10	STAT	Charge Status Output. Open Drain output. When target output voltage is reached, N-MOSFET turns on. This pin needs a pull up resistor.
11	FB	Feedback Voltage Pin.
12	VDD	Power Input Pin.
13, 14	SW	N-MOSFET Switching Node.
15, 16, 17 (Exposed Pad)	PGND	Power Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD} ---------- 6V
- Battery Input Voltage, V_{BAT} ---------- 12V
- Built-in N-Channel Enhancement MOSFET
  Drain-Source Voltage ---------- 50V
  SW Pulse Current (Pulse Width ≤ 1us) ---------- 4A
  SW Continuous Current ---------- 2A
  CS, VDOUT, FBVD, CHARGE, DRVIN, VDRV, DRVOUT, STAT, FB ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 1.67W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, θ_{JA} ---------- 60°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Built-in N-Channel Enhancement MOSFET
  Drain-Source Voltage ---------- 40V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 3.3V/5V, T_A = 25°C, unless otherwise specification)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
V_{DD} Operating Voltage	RT9594A	V_{DD}		3.15	3.3	3.4	V
	RT9594B			4.5	5	5.5	
Battery Voltage		V_{BAT}		1.6	--	9	V
Switch-Off Current (I_{VDD})		$I_{VDD\_SW\_OFF}$	V_{FB} = 1.1V	--	1	10	uA
Shutdown Current (I_{VDD})		I_{OFF}	CHARGE pin = 0V	--	0.01	1	uA
FB Voltage		V_{FB}		0.985	1	1.015	V
Line Regulation	RT9594A	$\lvert \Delta V_{FB} \rvert$	3.15V ≤ V_{DD} ≤ 3.4V	--	--	8	mV
	RT9594B		4.5V ≤ V_{DD} ≤ 5.5V				
STAT Open Drain $R_{DS(ON)}$				--	11	19	Ω
Charge Enable High		V_{CEH}		1.3	--	--	V
Charge Enable Low		V_{CEL}		--	--	0.4	V

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Built-in N-Channel Enhancement MOSFET							
Drain-Source On-Resistance	RT9594A	$R_{DS(ON)}$	I_D = 10mA	--	300	400	mΩ
	RT9594B			--	250	350	
Max Off Time During Pre-Charge				--	9	--	us
Min Off Time				--	400	--	ns
IGBT Driver							
IGBT Driver Supply Voltage		V_{VDRV}		2	--	5.5	V
DRVIN Trip Point				0.8	1.5	2.4	V
DRVOUT On Resistance to V_{VDRV}			V_{VDRV} = 3.3V	--	6	--	Ω
DRVOUT On Resistance to GND			V_{VDRV} = 3.3V	--	6	--	Ω
Propagation Delay (Rising)				--	20	--	ns
Propagation Delay (Falling)				--	200	--	ns
Voltage Detector							
Voltage Detector Trip (Falling)		V_{FBVD}	FBVD Falling	0.95	0.99	1.03	V
Voltage Detector Hysteresis		V_{FBVD_HYS}		--	65	--	mV
VDOUT on Resistance to GND				--	12	--	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

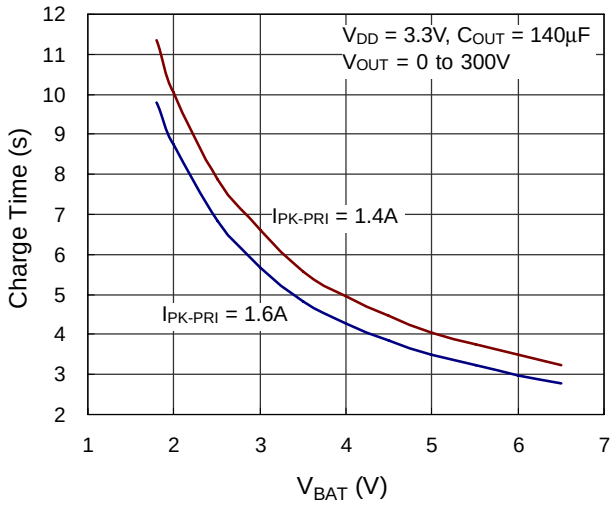
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board (single layer, 1S) of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

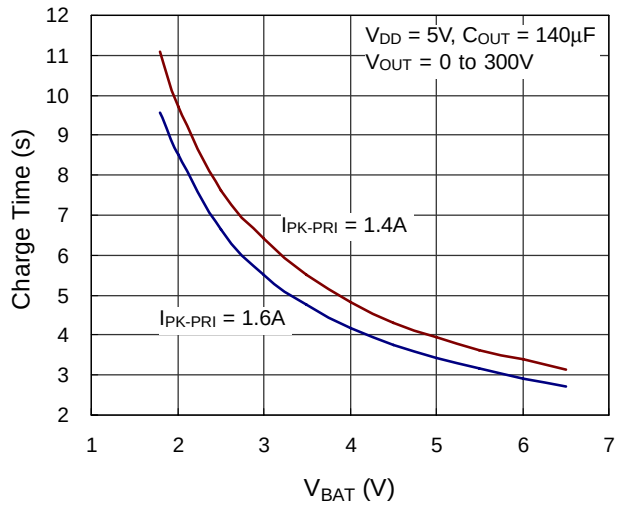
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

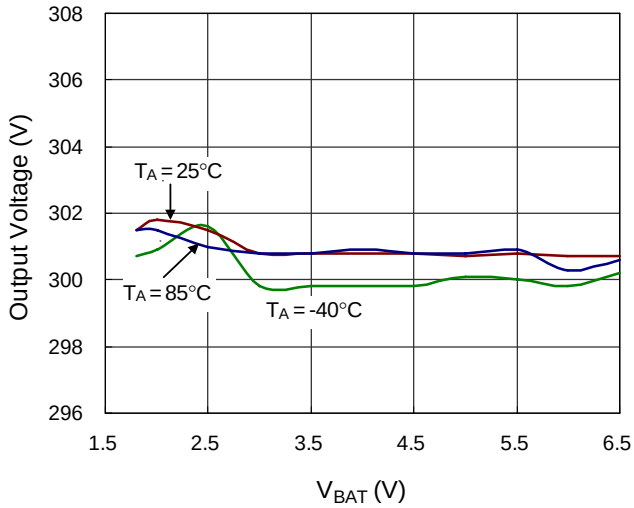
Charge Time vs. V_{BAT}



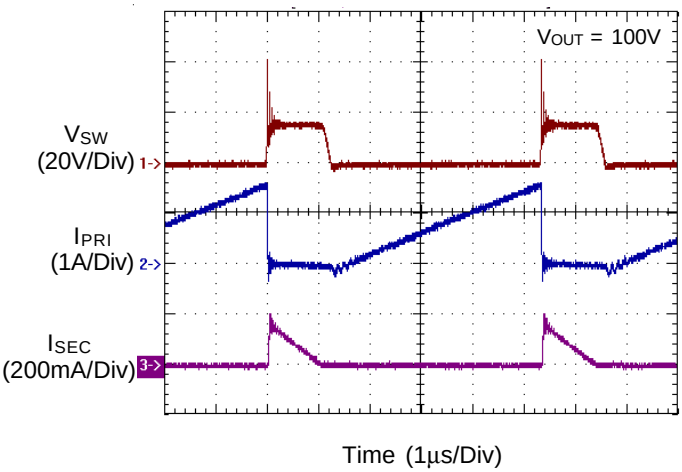
Charge Time vs. V_{BAT}



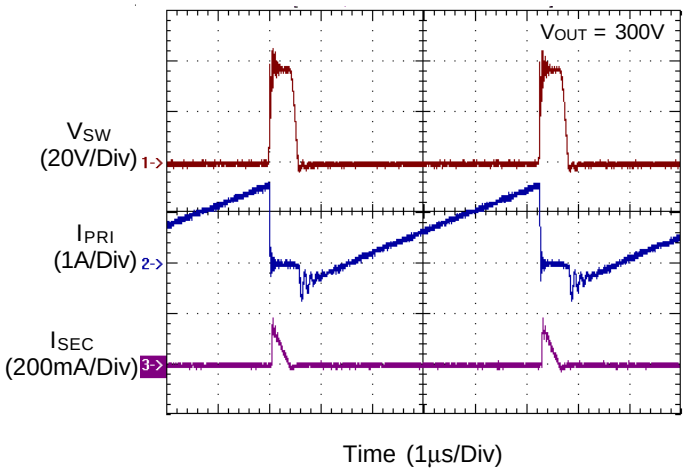
Output Voltage vs. V_{BAT}



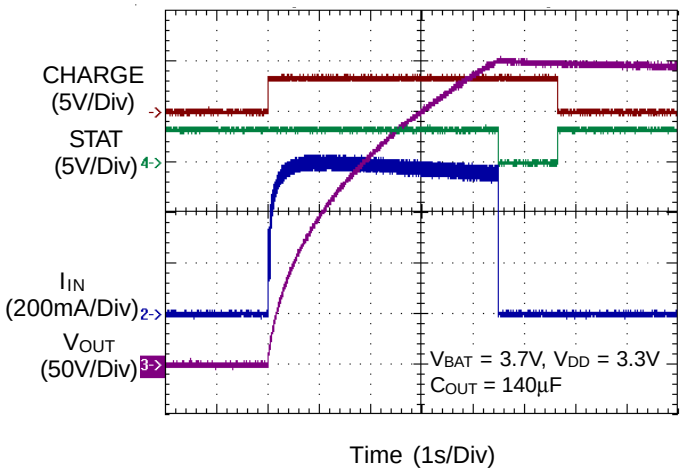
Switching



Switching



Charging



Application Information

The RT9594A/B integrate a constant peak current controller for charging photoflash capacitor and an IGBT driver for igniting flash tube.

The photoflash capacitor charger uses constant primary peak current and SW falling control to efficiently charge the photoflash capacitor. Pulling the CHARGE pin high will initiate the charging cycle. During MOS on period, the primary current ramps up linearly according to V_{BAT} and primary inductance. A resistor connecting from CS pin to GND determines the primary peak current.

During the MOS off period, the energy stored in the flyback transformer is boosted to the output capacitor. The secondary current decreases linearly at a rate determined by the secondary inductance and the output voltage (neglecting the voltage drop of the diode). The SW pin monitors the secondary current. When the secondary current drops to 0A, SW voltage falls then MOS on period starts again. The charging cycle repeats itself and charges the output capacitor.

The output voltage is sensed by a voltage divider connecting to the anode of the rectifying diode. When the output voltage reaches the desired voltage set by the resistor divider, the charging block will be disabled and stop charging. Then STAT pin will be pulled low to indicate the complete charging. The voltage-sensing path will be cut off when charging completed to minimize the output voltage decay. Both the CHARGE and STAT pins can be easily interfaced to a microprocessor in a digital system.

Transformer

The flyback transformer should be appropriately designed to ensure effective and efficient operation.

1. Turns Ratio

The turns ratio of transformer (N) should be high enough so that the absolute maximum voltage rating for the internal N-MOSFET drain to source voltage is not exceeded. Choose the minimum turns ratio according to the following formula :

$$N_{MIN} \geq \frac{V_{OUT}}{45 - V_{BAT}}$$

Where :

V_{OUT} : Target Output Voltage

V_{BAT} : Battery Voltage

2. Primary Inductance

For each switching cycle, energy transferred to the output capacitor is proportional to the primary inductance for a constant primary current. The higher the primary inductance is, the higher the charging efficiency will be. Besides, to ensure enough off time for output voltage sensing, the primary inductance should be high enough according to the following formula :

$$L_{PRI} \geq \frac{400 \times 10^{-9} \times V_{OUT}}{N \times I_{PK-PRI}}$$

V_{OUT} : Target Output Voltage

N : Transformer turns ratio

I_{PK-PRI} : Primary peak current

3. Leakage Inductance

The leakage inductance of the transformer results in the first spike voltage when N-MOSFET turns off. The spike voltage is proportional to the leakage inductance and inductor peak current. The spike voltage must not exceed the dynamic rating of the N-MOSFET drain to source voltage (50V).

4. Transformer Secondary Capacitance

Any capacitance on the secondary can severely affect the efficiency. A small secondary capacitance is multiplied by N^2 when reflected to the primary will become large. This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. Therefore, both the primary leakage inductance and secondary side capacitance should be minimized.

Rectifying Diode

The rectifying diode should be with short reverse recovery time (small parasitic capacitance). Large parasitic capacitance increases switching loss and lowers charging efficiency. In addition, the peak reverse voltage and peak current of the diode should be sufficient.

The peak reverse voltage of the diode is approximately :

$$V_{PK-R} \approx V_{OUT} + (N \times V_{BAT})$$

The peak current of the diode equal primary peak current divide transformer turn ratio as the following equation :

$$I_{PK-SEC} = \frac{I_{PK-PRI}}{N}$$

Where : N is transformer turns ratio.

Adjustable Input Current

The RT9594A/B simply adjust peak primary current by a resistor R_{CS} connecting to CS pin as shown in Function block diagram. R_{CS} determines the peak current of primary N-MOSFET according to the following Equation :

$$R_{CS} = \frac{40000}{I_{PK-PRI}} \quad (\Omega)$$

Where the I_{PK-PRI} is the primary peak current. Users could select appropriate R_{CS} according to the battery capability and required charging time.

Adjustable Output Voltage

The RT9594A/B sense output voltage by a voltage divider connecting to the anode of the rectifying diode during OFF time as shown in Figure 3. This eliminates power loss at voltage-sensing circuit when charging completed. R1 to R2 ratio determines the output voltage as shown in the typical application circuit. The feedback reference voltage is 1V. If V_{OUT} = 300V, according the following equation :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1+R2}{R3}\right), \text{ so } \frac{R1+R2}{R3} = 299.$$

It is recommend to set R3 = 1kΩ and R1 = R2 = 150kΩ for reducing parasitic capacitance coupling effect of the FB pin. R1 and R2 ***MUST*** be greater than 0805 size resistor for enduring secondary HV. Another sensing method is to sense the output voltage directly as shown in Figure 4.

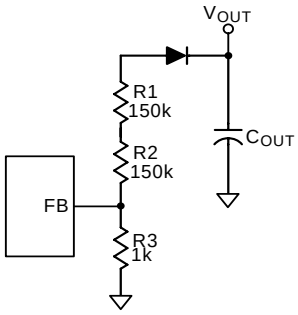


Figure 3. Sensing Anode of Diode

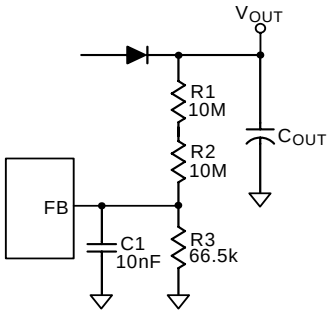


Figure 4. Sensing Output Voltage

Lower Charging Current at Low Battery Voltage

The RT9594A/B also offers two stage charging function. If the resistor divider is connected from V_{BAT} to FBVD to GND as shown in Figure 5, it will detect the battery voltage. Because of the reference voltage of the internal detector is 1V, thus the battery trip point is 2.5V. When battery voltage is >2.5V, the VDOUT open drain MOS inside the RT9594A/B will be turned on (VDOUT state become GND), the peak current value will be determined by R4. When battery voltage is <2.5V, the VDOUT open drain MOS inside the RT9594A/B will be turned off (VDOUT state become OPEN), then the peak current is determined by R4 series with R5. Thus charging current is decreasing as shown in Figure 7.

As shown in the Figure 6 circuit, the FBVD voltage also could be set by the GPIO signal. When GPIO voltage is >1V, the first stage peak current value will be determined by R4. When the GPIO voltage is <1V, the second stage peak current is determined by R4 series with R5.

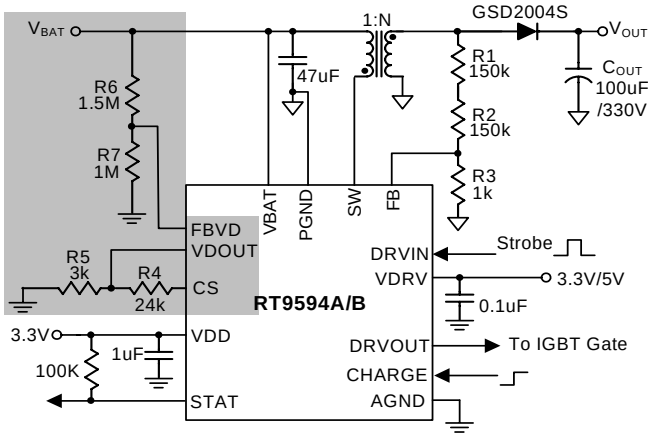


Figure 5. Two Stage Charging Application Circuit

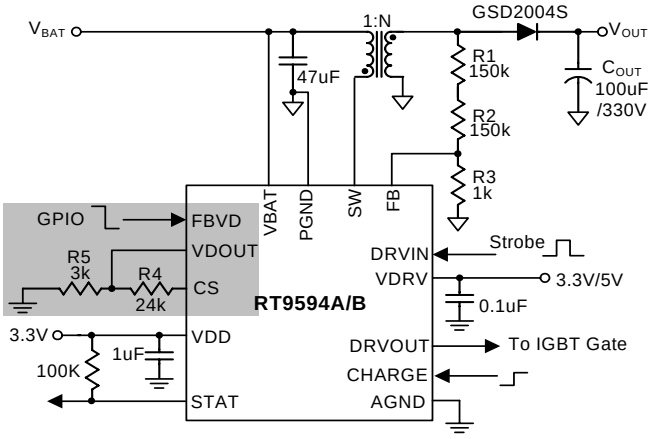


Figure 6. Two Stage Charging by GPIO Signal

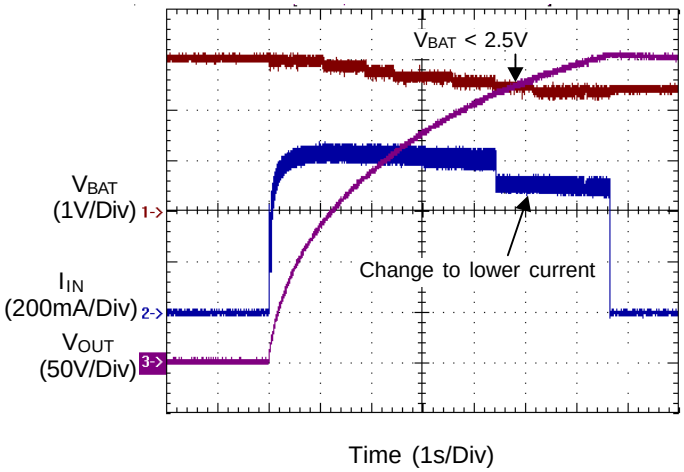


Figure 7. Lower Charging Current

Layout Guide

For best performance, careful PCB layout is necessary. The following guidelines should be strictly followed when designing a PCB layout for the RT9594A/B.

1. Both of primary and secondary power paths should be as short as possible.
2. Place the R_{CS} as close to chip as possible. The GND side of R_{CS} should be directly connected to ground plane to avoid noise coupling.
3. Keep FB node area small and far away from nodes with voltage switching to reduce parasitic capacitance coupling effect.
4. The PGND should be connected to V_{BAT} ground plane to reduce switching noise.

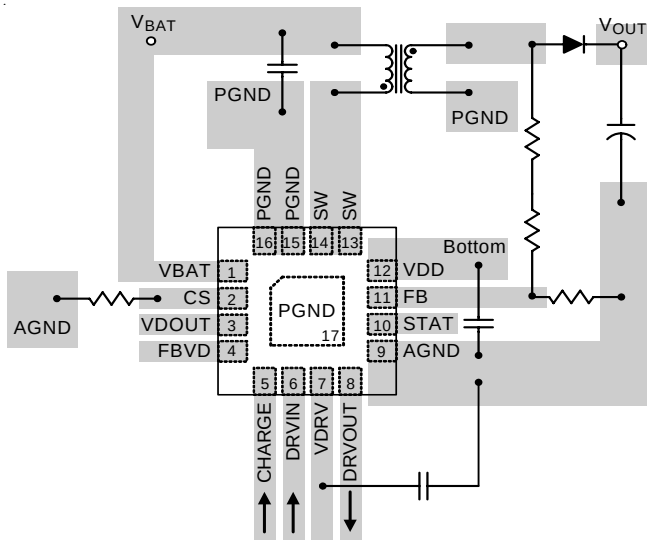
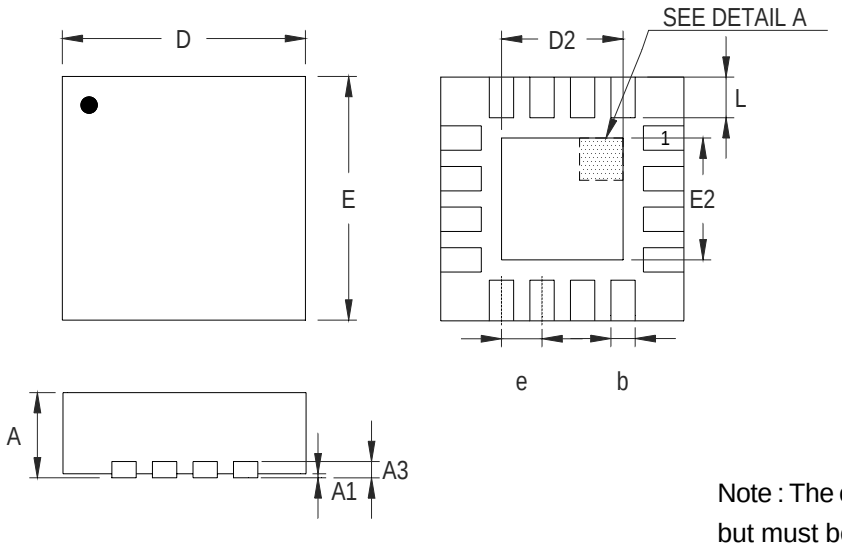
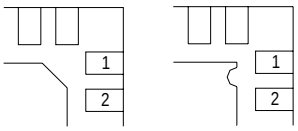


Figure 8. Suggestion Layout

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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