12V Synchronous Buck PWM DC/DC and Linear Power Controller

General Description

The RT9259 is a dual-channel DC/DC controller specifically designed to deliver high quality power where 12V power source is available. This part consists of a synchronous buck controller and an LDO controller. The synchronous buck controller integrates MOSFET drivers that support 12V + 12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count. The LDO controller drives an external N-MOSFET for lower power requirement.

Other features include adjustable operation frequency, internal soft start, under voltage protection, over current protection and shut down function. With the above functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solution. This part comes to VQFN-16L 4x4, SOP14 and SSOP-16 packages.

Ordering Information

RT9259 □ □

- Package Type
  - S : SOP-14
  - A : SSOP-16
  - QV : VQFN-16 4x4 (V-Type)
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

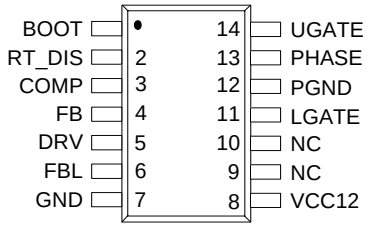
- **Single 12V Bias Supply**
- **Support Dual Channel Power Conversion**
  - **One Synchronous Rectified Buck PWM Controller**
  - **One Linear Controller**
- **Both Controllers Drive Low Cost N-MOSFETs**
- **Adjustable Frequency from 150kHz to 1MHz and Free-Run Frequency at 230kHz**
- **Small External Component Count**
- **Output Voltage Regulation**
  - **PWM Controller : ±1% Accuracy**
  - **LDO Controller : ±2% Accuracy**
- **Two Internal V_{REF} Power Support Lower to 0.8V**
- **Adjustable External Compensation**
- **Linear Controller Drives N-MOSFET Pass Transistor**
- **Fully-Adjustable Outputs**
- **Under Voltage Protection for Both Outputs**
- **Over Current Fault Monitor on MOSFET; No Current Sense Resistor is Required**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

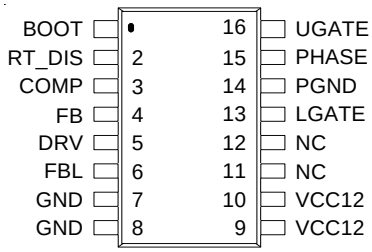
- Graphic Card GPU, Memory Core Power
- Graphic Card Interface Power
- Motherboard, Desktop and Servers Chipset and Memory Core Power
- IA Equipments
- Telecomm Equipments
- High Power DC/DC Regulators

Pin Configurations

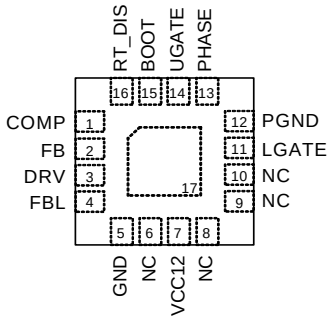
(TOP VIEW)



SOP-14



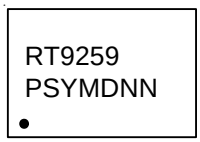
SSOP-16



VQFN-16L 4x4

Marking Information

RT9259PS

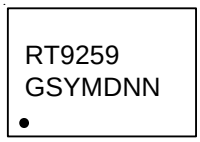


RT9259PS : Product Number
YMDNN : Date Code

RT9259PA

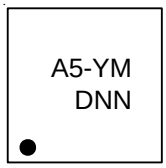
RT9259PA : Product Number
YMDNN : Date Code

RT9259GS



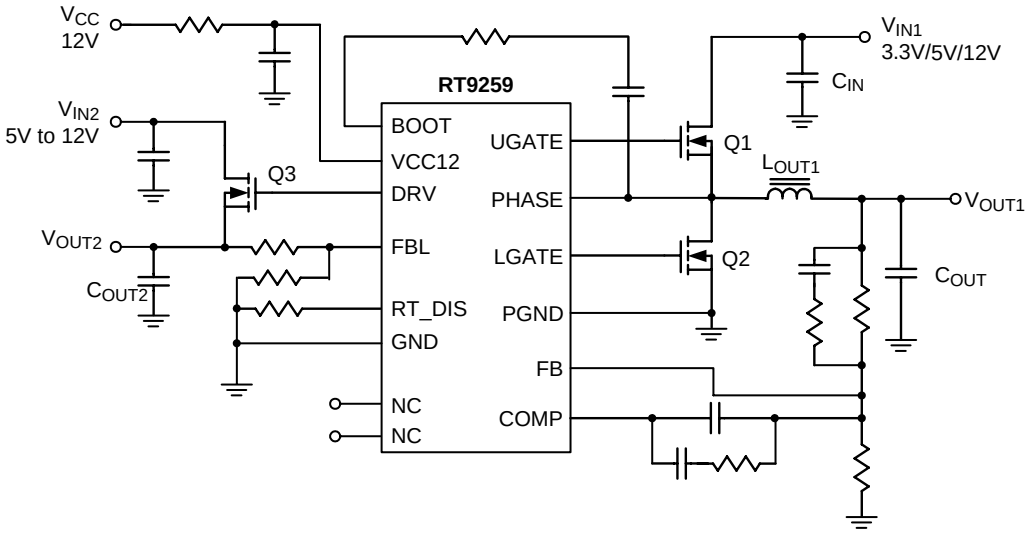
RT9259GS : Product Number
YMDNN : Date Code

RT9259PQV



A5- : Product Code
YMDNN : Date Code

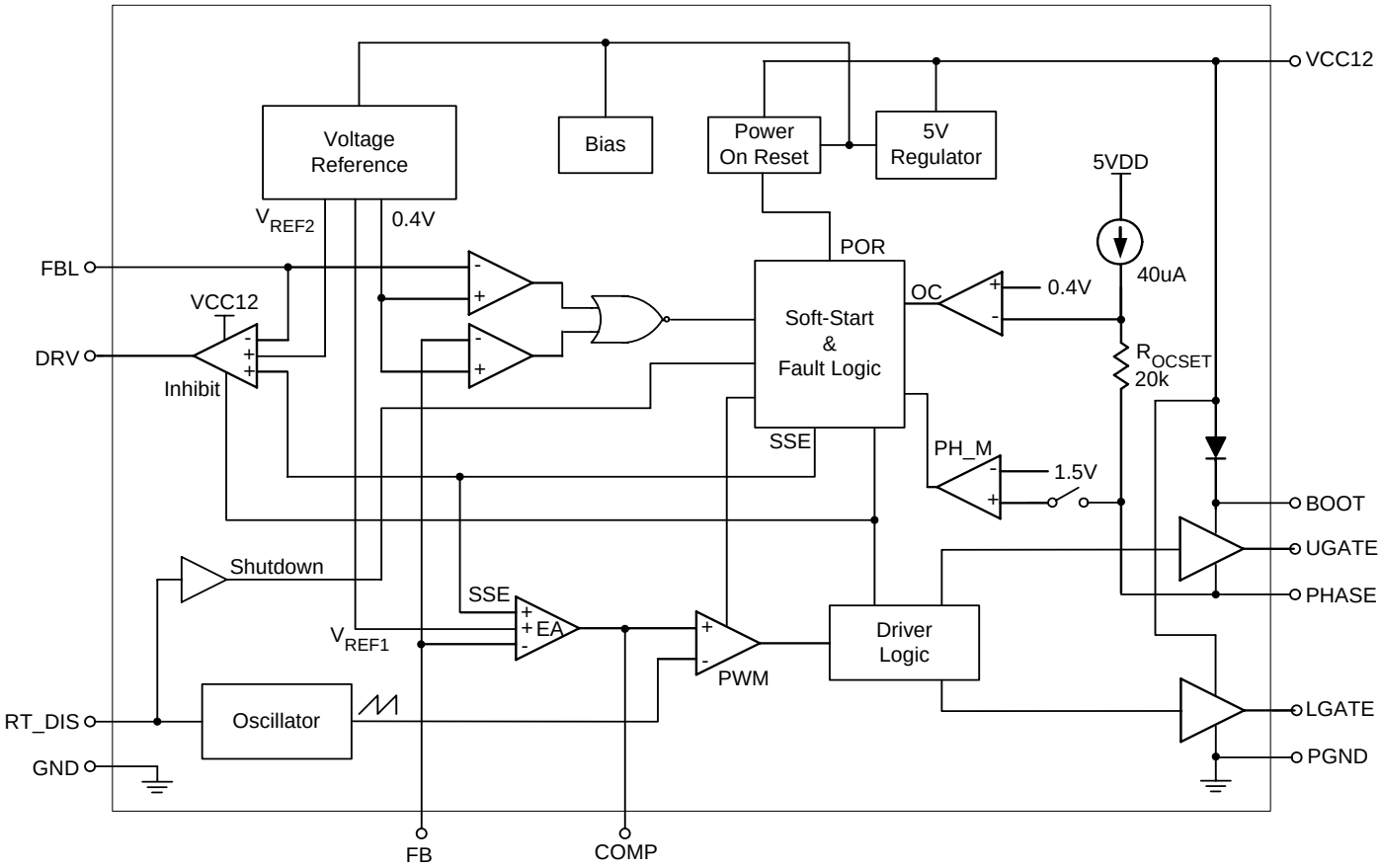
Typical Application Circuit



Functional Pin Description

Pin No.			Pin Name	Pin Function
RT9259□S	RT9259□A	RT9259PQV		
1	1	15	BOOT	Bootstrap supply for the upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
2	2	16	RT_DIS	Connect a resistor from RT_DIS to GND to set frequency. In addition, if this pin is pulled down towards GND, it will disable both regulator outputs until released.
3	3	1	COMP	Buck converter external compensation. This pin is used to compensate the control loop of the buck converter.
4	4	2	FB	Buck converter feedback voltage. This pin is the inverting input of the PWM error amplifier. FB senses the switcher output through an external resistor divider network.
5	5	3	DRV	Connect this pin to the gate of an external MOSFET. This pin provides the drive for the linear regulator's pass MOSFET.
6	6	4	FBL	Linear regulator feedback voltage. This pin is the inverting input of the LDO error amplifier and protection monitor. Connect this pin to an external resistor divider network of the linear regulator.
7	7, 8	5	GND	Ground.
8	9, 10	7	VCC12	Connect this pin to a well-decoupled 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.
9, 10	11, 12	6, 8, 9, 10, 17 (Exposed Pad)	NC	No Internal Connection.
11	13	11	LGATE	Lower gate driver output. Connect to the gate of the low-side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
12	14	12	PGND	Power ground return for the lower gate driver.
13	15	13	PHASE	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
14	16	14	UGATE	Connect this pin to a well-decoupled 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 15V
- BOOT to PHASE ---------- –0.3V to 15V
- PHASE to GND
  - DC ---------- –0.3V to 15V
  - < 20ns ---------- –5V to 30V
- LGATE to GND
  - DC ---------- (GND – 0.3V) to (VCC + 0.3V)
  - < 20ns ---------- (GND – 5V) to (VCC + 5V)
- UGATE to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 20ns ---------- (V_{PHASE} – 5V) to (V_{BOOT} + 5V)
- PWM to GND ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-14 ---------- 1.000W
  - SSOP-16 ---------- 0.909W
  - VQFN-16L 4x4 ---------- 1.852W
- Package Thermal Resistance (Note 2)
  - SOP-14, θ_{JA} ---------- 100°C/W
  - SSOP-16, θ_{JA} ---------- 110°C/W
  - VQFN-16L 4x4, θ_{JA} ---------- 54°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Power Supply Voltage	V_{CC}		--	12	15	V
Power On Reset	V_{VCCRTH}	V_{CC} Rising	8.8	9.6	10.4	V
Power On Reset Hysteresis	V_{VCCHYS}		0.4	0.78	1.2	V
Power Supply Current	I_{VCC}	UGATE, LGATE Open	--	3	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Free Running Frequency	f_{OSC}	R_{RT} = 110kΩ	250	300	350	kHz
Ramp Amplitude			--	1.6	--	V
Reference Voltage						
PWM Error Amplifier Reference	V_{REF1}		0.792	0.8	0.808	V
Linear Driver Reference	V_{REF2}		0.784	0.8	0.816	V
Error Amplifier						
DC Gain			70	88	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	6	15	--	MHz
Slew Rate	SR		3	6	--	V/μs
Gate Driver						
Upper Drive Source	R_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{BOOT} - V_{UGATE}$ = 1V	--	4	8	Ω
Upper Drive Sink	R_{UGATE}	V_{UGATE} = 1V	--	4	8	Ω
Lower Drive Source	R_{LGATE}	$V_{CC} - V_{LGATE}$ = 1V	--	4	6	Ω
Lower Drive Sink	R_{LGATE}	V_{LGATE} = 1V	--	2	4	Ω
Protection						
Under Voltage Protection	V_{UVP}		0.36	0.4	0.45	V
Soft-Start Time Interval	T_{SS}		2	3	4	ms
Over Current Threshold	V_{OC}		--	–400	--	mV
RT_DIS Shutdown Threshold			0.35	0.4	--	V
Linear Regulator						
Output High Voltage	V_{DRV}		9.5	10.3	--	V
Output Low Voltage	V_{DRV}		--	0.1	1	V
Source Current	I_{DRVSR}		2	--	--	mA
Sink Current	I_{DRVSC}		0.5	--	--	mA

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

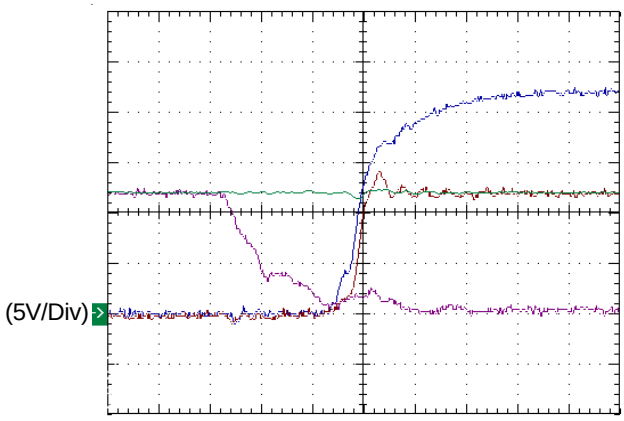
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

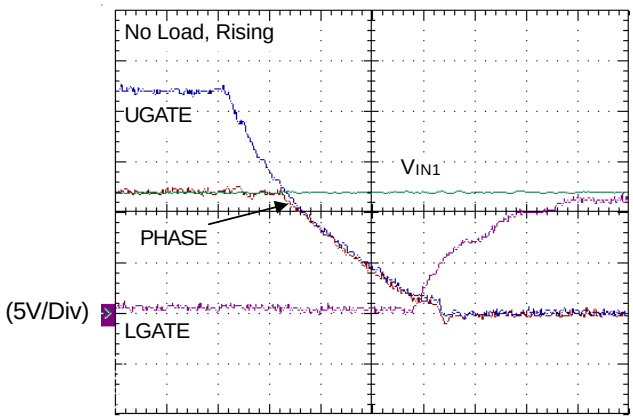
Typical Operating Characteristics

Dead Time



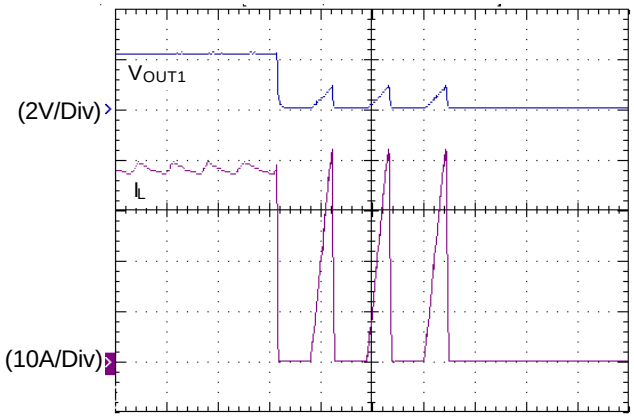
Time (25ns/Div)

Dead Time



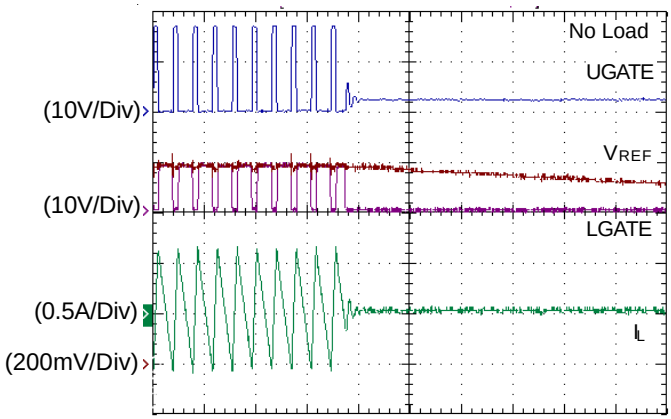
Time (25ns/Div)

OCP



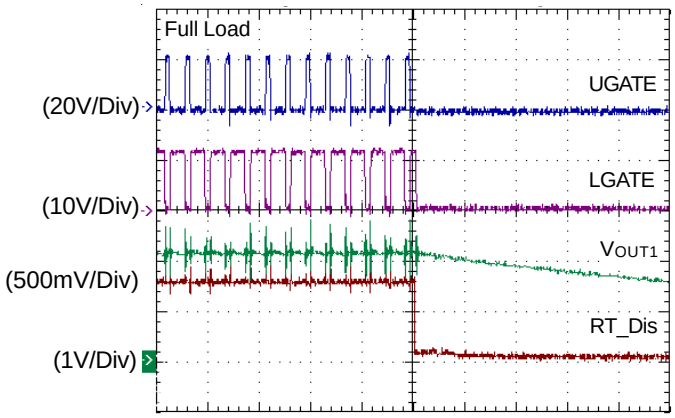
Time (2.5ms/Div)

Power Off



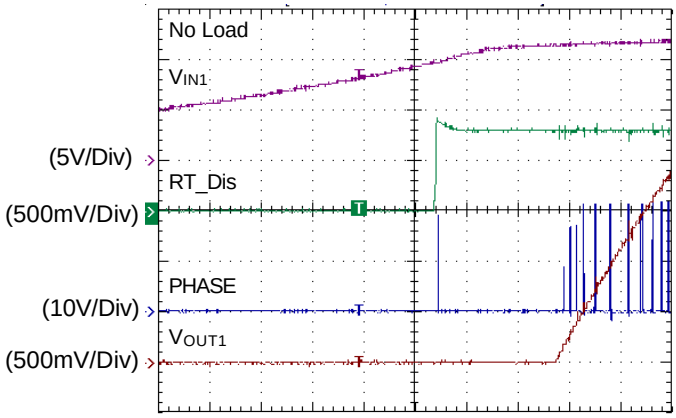
Time (5µs/Div)

Shut Down



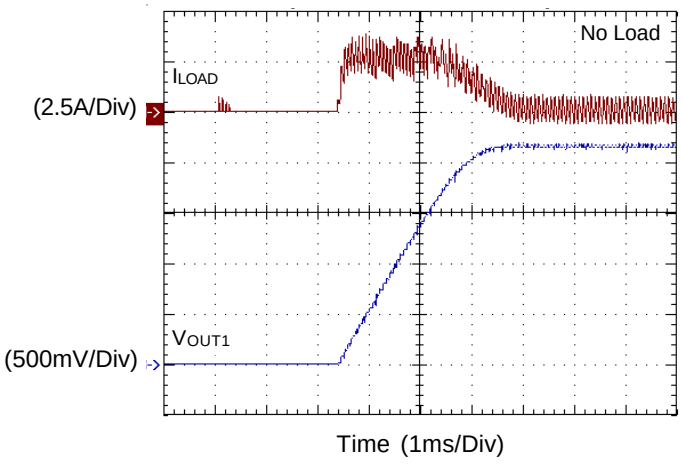
Time (5µs/Div)

Start Up

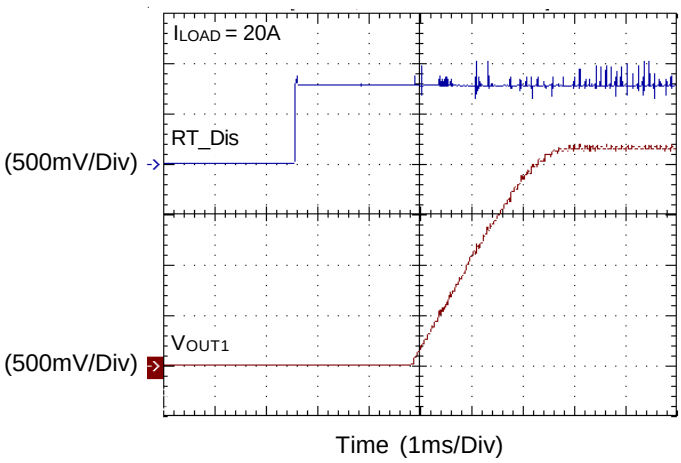


Time (1ms/Div)

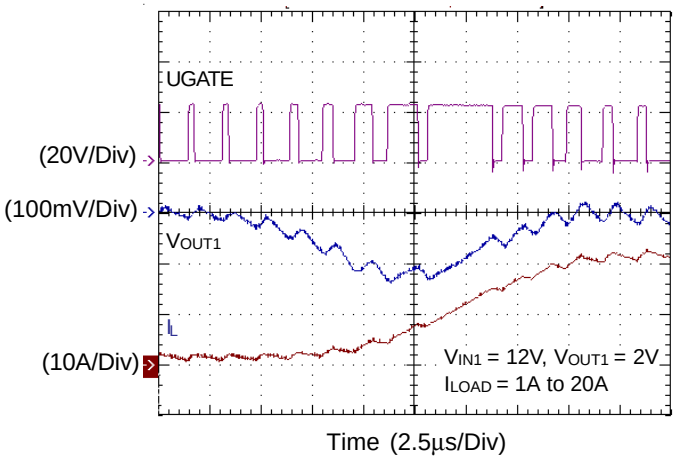
Start Up



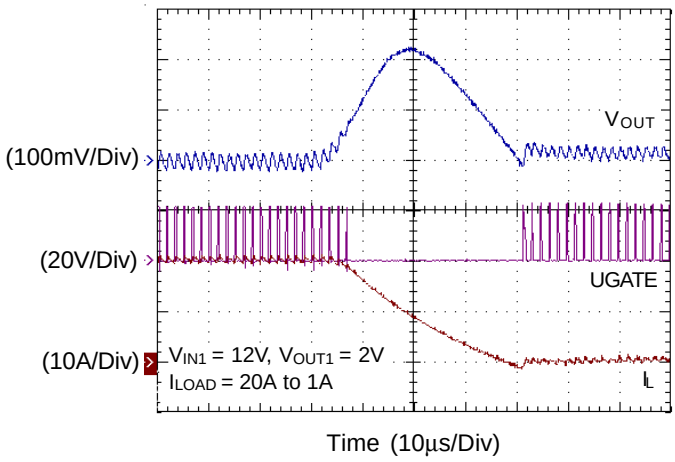
Start Up



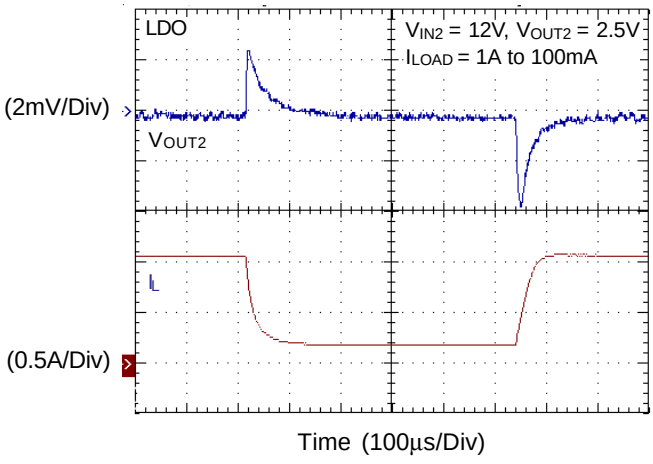
Transient Response



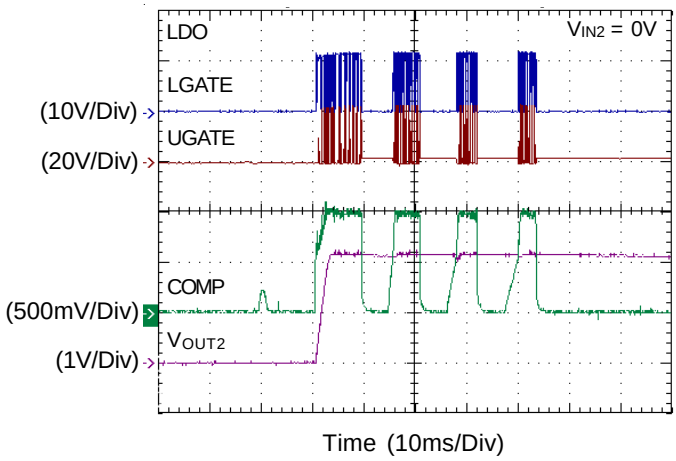
Transient Response



Transient Response



Under Voltage Protection



Application Information

Introduction

The RT9259 is a dual-channel DC/DC controller specifically designed to deliver high quality power where 12V power source is available. This part consists of a synchronous buck controller and an LDO controller. The synchronous buck controller integrates internal MOSFET drivers that support 12V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count. The LDO controller drives an external N-MOSFET for lower power requirement.

Internal 5VDD Regulator

It is highly recommended to power the RT9259 with well-decoupled 12V to VCC12 pin. VCC12 powers the RT9259 control circuit, low side gate driver and bootstrap circuit for high side gate driver. A bootstrap diode is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required. The RT9259 integrates MOSFET gate drives that are powered from the VCC12 pin and support 12V + 12V driving capability. Converters that consist of RT9259 feature high efficiency without special consideration on the selection of MOSFETs.

An internal linear regulator regulates VCC12 input to a 5VDD voltage for internal control logic circuit. No external bypass capacitor is required for filtering the 5VDD voltage. This further facilitates PCB design and reduces the total BOM cost.

Power On Reset

The RT9259 automatically initializes upon applying input power (at the VCC12) pin. The power on reset function (POR) continually monitors the input bias supply voltage at the VCC12 pin. The VCC12V POR level is typically 9.6V at VCC12V rising.

Frequency Setting and Shut Down

Connecting a resistor R_{RT} from the RT_DIS pin to GND sets the operation frequency. The relation can be roughly expressed in the equation.

$$f_{OSC} \cong 230kHz + \frac{7700}{R_{RT}}(kHz)$$

When let open, the free running frequency is 230kHz typically. Figure 1 shows the operation frequency vs. R_{RT} for quick reference.

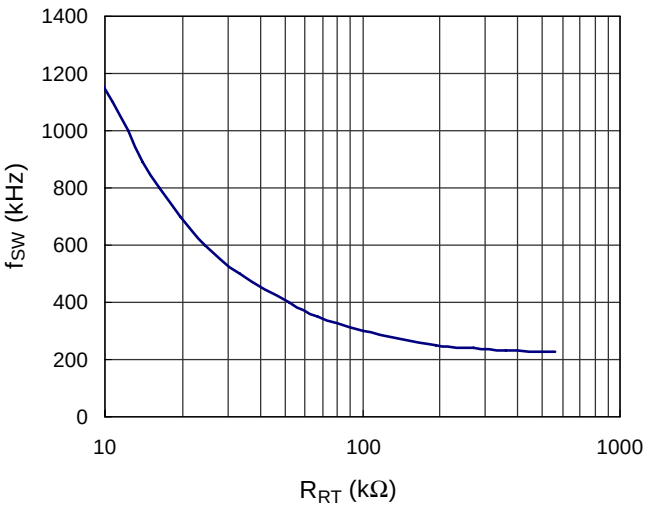


Figure 1. RT vs. fsw at Low Frequency

Shorting the RT_DIS pin to GND with an external signal-level MOSFET shuts down the device. This allows flexible power sequence control for specified application. The RT_DIS pin threshold voltage is 0.4V typically.

VIN1 Detection

The RT9259 continuously generates a 10kHz pulse train with 1μs pulse width to turn on the upper MOSFET for detecting the existence of VIN1 after VCC12V POR and RT_DIS enabled as shown in Figure 2. PHASE pin voltage is monitored during the detection duration.

If the PHASE voltage crosses 1.5V four times, VIN1 existence is recognized and the RT9259 initiates its soft start cycle as described in next section.

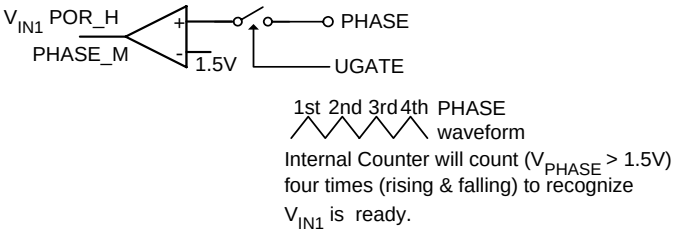


Figure 2

Soft Start for Synchronous Buck Converter

A built-in soft-start is used to prevent surge current from power supply input during power on (referring to the Functional Block Diagram). The error amplifier EA is a three-input device. SSE or V_{REF1} whichever is smaller dominates the behavior non-inverting input. The internal soft start voltage SSE linearly ramps up to about 4V after VIN1 existence is recognized with about 2ms delay. According, the output voltage ramps up smoothly to its target level. The rise time of output voltage is about 2ms as shown in Figure 3. V_{REF1} takes over the behavior EA when SSE > V_{REF1}.

SSE is also used for LDO soft start. LDO input voltage VIN2 ***MUST*** be ready before SSE starts to ramp up. Otherwise UVP function of LDO may be triggered and shut down the RT9259.

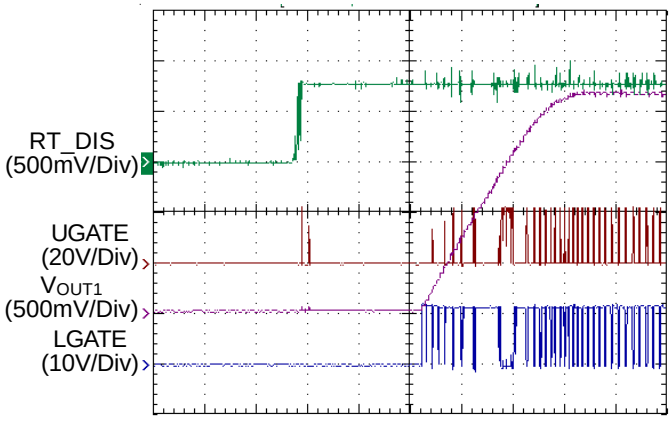


Figure 3 : Start up by RT_DIS

Under Voltage Protection

The voltages at FB and FBL pin are monitored for under voltage protection (UVP) after the soft start is completed. UVP is triggered if one of the feedback voltages is under (50% x V_{REFX}) with a 30us delay. As shown in Figure 4, the RT9259 PWM controller is shut down when V_{FB} drops lower than the UVP threshold. In Figure 5, the RT9259 shuts down after 4 time UVP hiccups triggered by FBL.

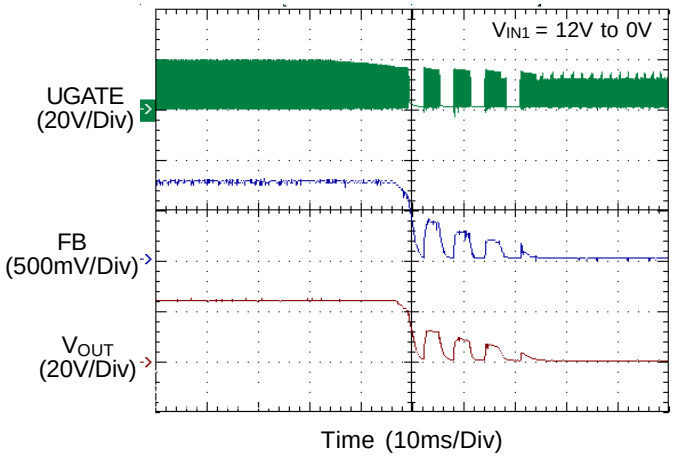


Figure 4. UVP triggered by FB

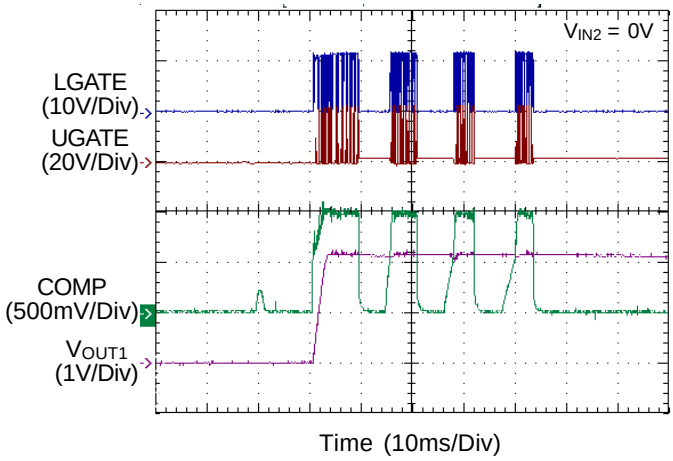


Figure 5. UVP hiccups triggered by FBL

Over Current Protection

The RT9259 senses the current flowing through lower MOSFET for over current protection (OCP) by sensing the PHASE pin voltage as shown in the Functional Block Diagram. A 40µA current source flows through internal 20kΩ R_{OCSET} to PHASE pin causes 0.8V voltage drop across the resistor. OCP is triggered if the voltage at PHASE pin (drop of lower MOSFET V_{DS}) is lower than –0.4V when low side MOSFET conducting. Accordingly inductor current threshold for OCP is a function of conducting resistance of lower MOSFET $R_{DS(ON)}$ as :

$$I_{OCSET} = \frac{40\mu A \times R_{OCSET}(20k\Omega) - 0.4V}{R_{DS(ON)}} = \frac{0.4V}{R_{DS(ON)}}$$

If MOSFET with $R_{DS(ON)}$ = 16mΩ is used, the OCP threshold current is about 25A. Once OCP is triggered, the RT9259 enters hiccup mode and re-soft starts again. The RT9259 shuts down after 4 time OCP hiccups.

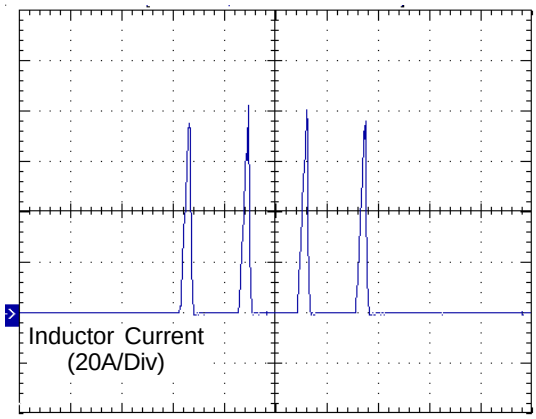


Figure 6. Shorted then Start Up

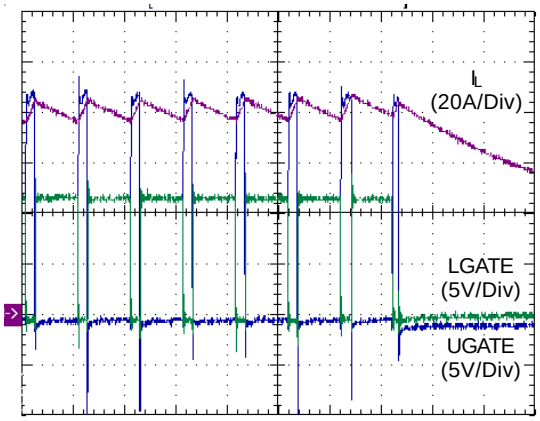


Figure 7. Shorted then Start Up (Extended Figure 3)

Feedback Compensation

The RT9259 is a voltage mode controller. The control loop is a single voltage feedback path including a compensator and modulator as shown Figure 8. The modulator consists of the PWM comparator and power stage. The PWM comparator compares error amplifier EA output (COMP) with oscillator (OSC) sawtooth wave to provide a Pulse-Width Modulated (PWM) with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier.

A well-designed compensator regulates the output voltage to the reference voltage V_{REF} with fast transient response and good stability.

In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (greater than 45 degrees) and the highest 0dB crossing frequency. It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of –20dB/dec.

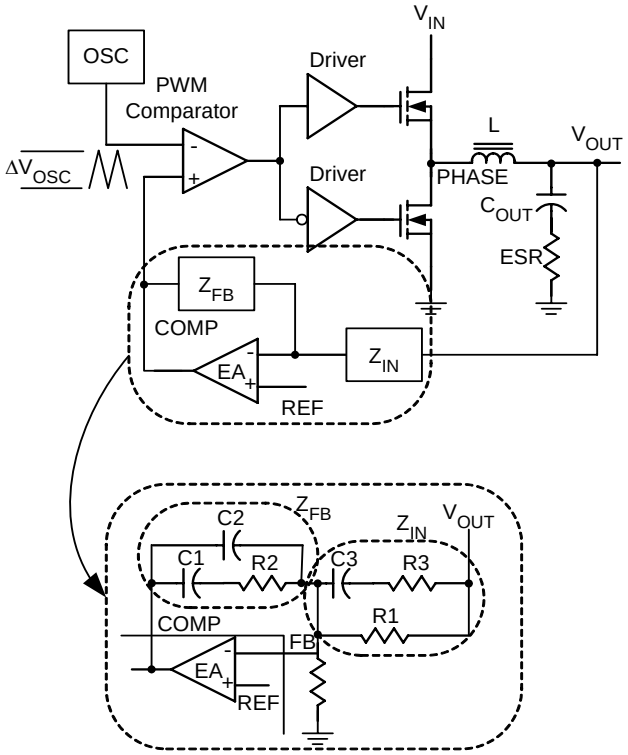


Figure 8. Closed Loop

1) Modulator Frequency Equations

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output. This transfer function is dominated by a DC gain, a double pole, and a zero as shown in Figure 10. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak to peak oscillator voltage V_{OSC}. The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter expressed as :

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor expressed as follows :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

2) Compensation Frequency Equations

The compensation network consists of the error amplifier and the impedance networks Z_C and Z_F as shown in Figure 9.

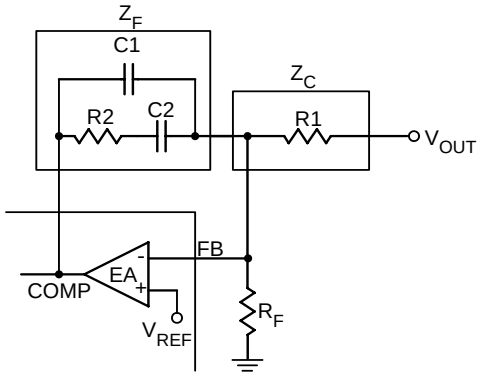


Figure 9. Compensation Loop

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

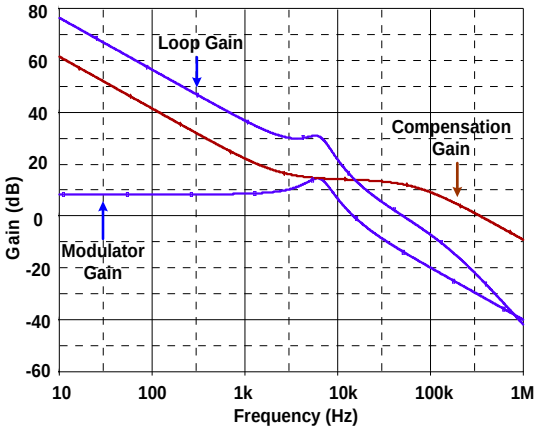


Figure 10. Bode Plot

Figure 10 shows the DC/DC converter's gain vs. frequency. The compensation gain uses external impedance networks Z_C and Z_F to provide a stable, high bandwidth loop. High crossover frequency is desirable for fast transient response, but often jeopardize the system stability. In order to cancel one of the LC filter poles, place the zero before the LC filter resonant frequency. In the experience, place the zero at 75% LC filter resonant frequency. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The second pole is placed at half the switching frequency.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For VQFN-16L 4x4 packages, the thermal resistance θ_{JA} is 54°C/W on the standard JEDEC 51-7 four-layers thermal test board.

The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / 54°C/W = 1.852 W for QFN-16L 4x4 packages

$P_{D(MAX)}$ = (125°C – 25°C) / 100°C/W = 1.000 W for SOP-14 packages

$P_{D(MAX)}$ = (125°C – 25°C) / 110°C/W = 0.909 W for SSOP-16 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance θ_{JA}. The Figure 11 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

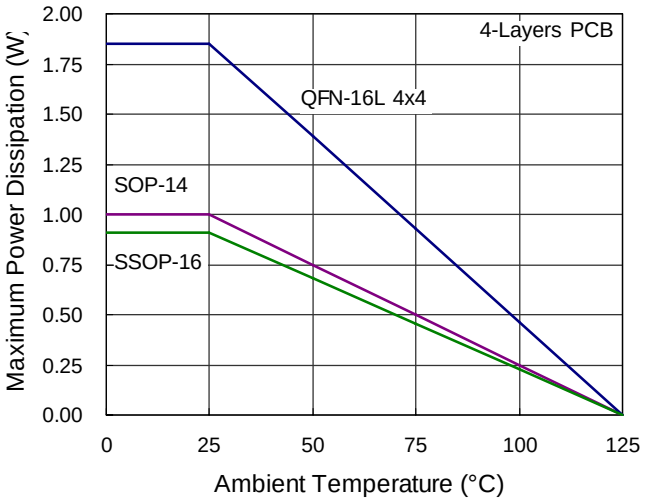


Figure 11. Derating Curve of Maximum Power Dissipation

Layout Consideration

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise, that results in over-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. Consider, as an example, the turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET or schottky diode.

Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using the RT9259. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near by MOSFETs. A multi-layer printed circuit board is recommended. Figure 12 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each of them represents numerous physical capacitors.

Use a dedicated grounding plane and use vias to ground all critical components to this layer. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node, but it is not necessary to oversize this particular island. Since the PHASE node is subjected to very high dV/dt voltages, the stray capacitance formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal routing. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

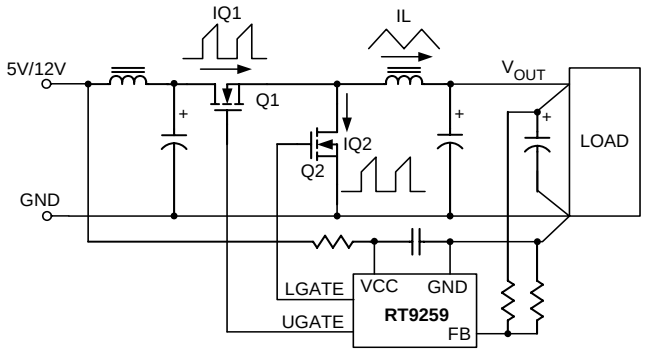
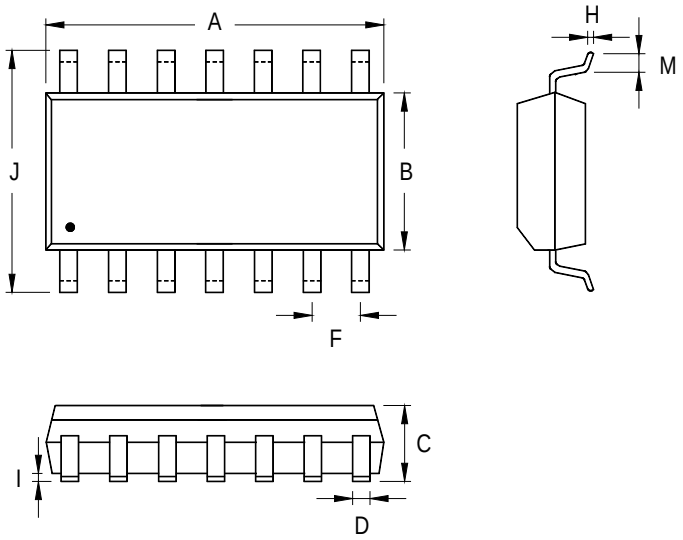


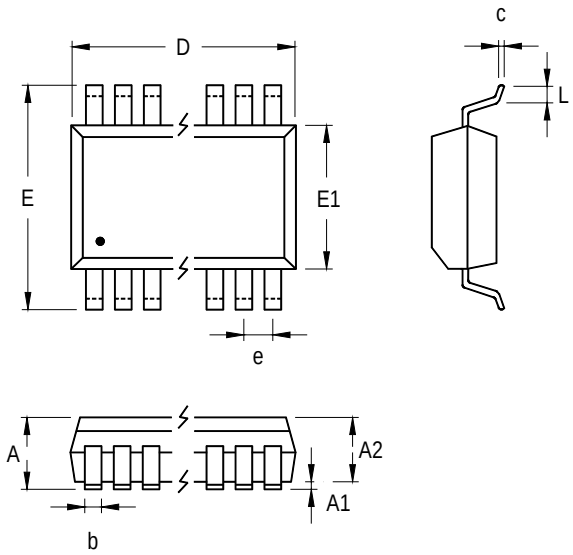
Figure 12. The Connections of the Critical Components in the Converter

Outline Dimension



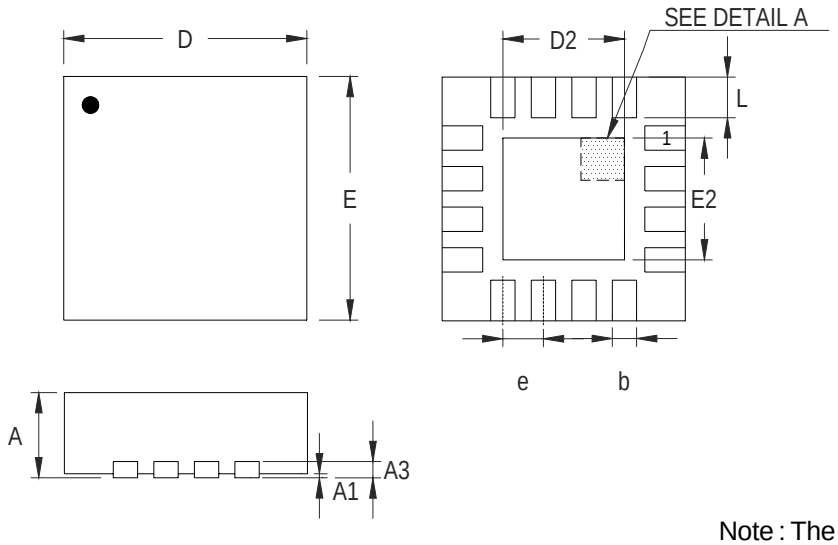
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

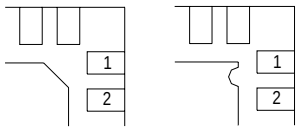
14-Lead SOP Plastic Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.346	1.753	0.053	0.069
A1	0.102	0.254	0.004	0.010
A2	1.499		0.059	
b	0.203	0.305	0.008	0.012
C	0.178	0.254	0.007	0.010
D	4.801	5.004	0.189	0.197
e	0.635		0.025	
E	5.791	6.198	0.228	0.244
E1	3.810	3.988	0.150	0.157
L	0.406	1.270	0.016	0.050

16-Lead SSOP Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.380	0.010	0.015
D	3.950	4.050	0.156	0.159
D2	2.000	2.450	0.079	0.096
E	3.950	4.050	0.156	0.159
E2	2.000	2.450	0.079	0.096
e	0.650		0.026	
L	0.500	0.600	0.020	0.024

V-Type 16L QFN 4x4 Package

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