5V/12V Single Synchronous Buck PWM Controller

General Description

The RT8116 is a low cost PWM controller with an integrated N-MOSFET gate driver for a single synchronous buck converter. The highly integrated 8-pin controller reduces size and cost of the power supply. The RT8116 can be used in a wide variety of applications, since it can work with either 5V or 12V supplies. It provides single feedback loop, voltage mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V. Switching frequency is internally set at either 275kHz or 200kHz to save external component. The RT8116 also supports programmable soft-start function via an external capacitor. Protection features include programmable over current protection and under-voltage lockout (UVLO).

Ordering Information

RT8116 □□□

- Package Type
  - S : SOP-8
  - SP : SOP-8 (Exposed-Pad-Option 1)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- A : 275kHz
  - B : 200kHz

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8116 GSYMDNN ●	RT8116GS : Product Number YMDNN : Date Code
RT8116 GSPYMDNN ●	RT8116GSP : Product Number YMDNN : Date Code

Features

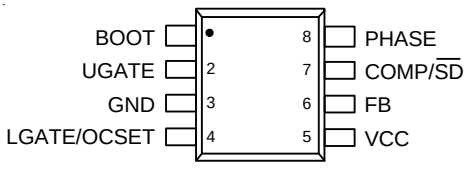
- **4.5V to 13.2V Supply Voltage Range**
- **Voltage Mode PWM Control**
- **Single Buck PWM Controller with Integrated N-MOSFET Driver**
- **Integrated Boot-Strapped Diode**
- **0.8V ±1% Internal Reference**
- **Internally Fixed Frequency at 275kHz or 200kHz**
- **Capacitor Programmable Soft-Start**
- **Enable/Shutdown Control On COMP/$\overline{SD}$ Pin**
- **85% Maximum Duty Cycle**
- **Over Current Protection with Lossless Lower MOSFET $R_{DS(ON)}$**
- **Input Under Voltage Lockout Protection**
- **Under Voltage Protection**
- **Pinless LGATE Over Current Protection Setting (LGOCS)**
- **RoHS Compliant and Halogen Free**

Applications

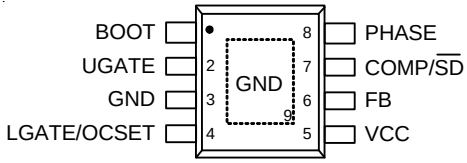
- Desktop Computers
- Graphic Cards
- 3.3V to 12V Input DC/DC Regulators
- Low Voltage Distributed Power Supplies

Pin Configurations

(TOP VIEW)

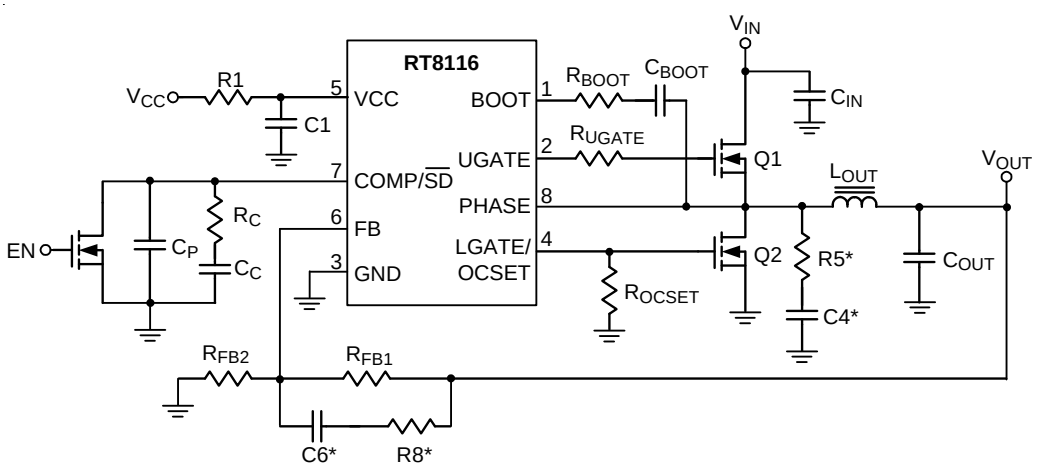


SOP-8



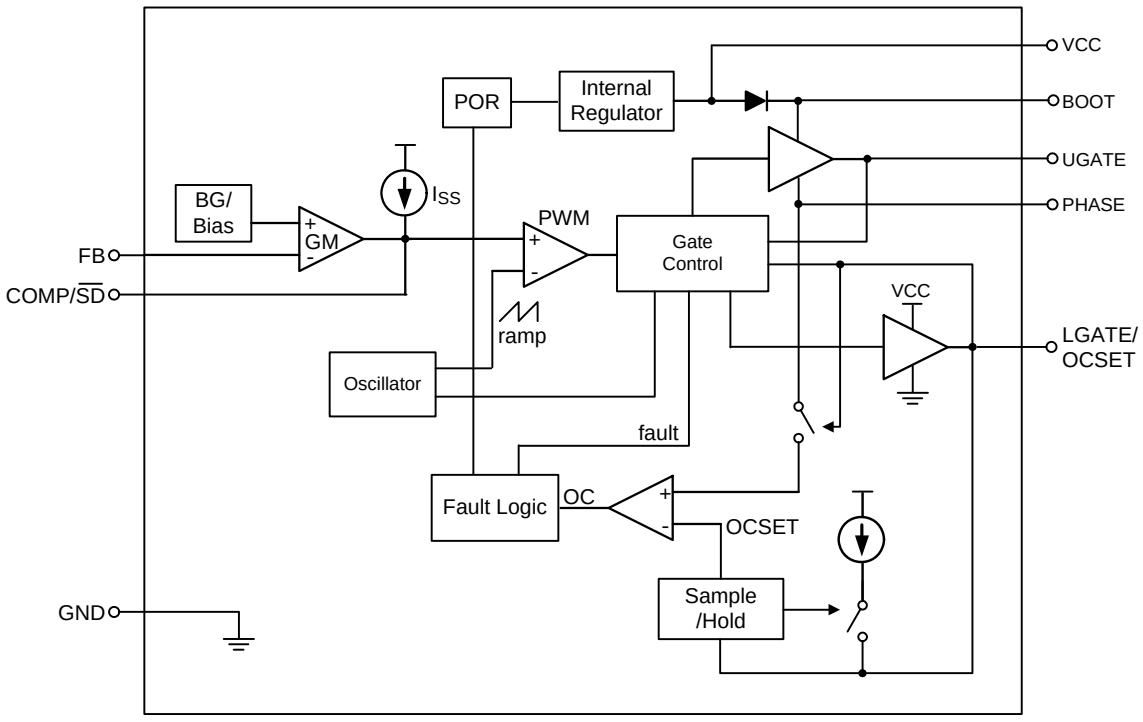
SOP-8 (Exposed Pad)

Typical Application Circuit



* : Optional

Function Block Diagram



Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-8	SOP-8 (Exposed Pad)		
1	1	BOOT	Bootstrap Supply Pin for Upper Gate Driver. Connect the bootstrap capacitor between BOOT pin and the PHASE on the upper MOSFET.
2	2	UGATE	Upper Gate Driver Output. Connect this pin to gate of the high side N-Channel power MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET is turned off.
3	3, 9 (Exposed Pad)	GND	Ground. Acts as both signal and power ground for the IC. All voltage levels are measured with respect to this pin. Ties the pin directly to the low-side MOSFET source and ground plane with the lowest impedance. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	4	LGATE/ OCSET	Lower gate Driver Output and OCP Set Pin. Connect this pin to the gate of the lower MOSFET; it provides the PWM-controlled gate drive (from VCC). This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET is turned off. During a short period of time following Power On Reset (POR) or shut down release, this pin is also used to determine the over current threshold of the converter. Connect a resistor (R_{OCSET}) from this pin to GND. See the over current protection section for equations.
5	5	VCC	Power Supply Pin. Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.
6	6	FB	Feedback Voltage Pin. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external voltage divider network.
7	7	COMP/$\overline{SD}$	Feedback Compensation Pin. This multiplexed pin can also be used as the $\overline{SD}$ pin. When COMP voltage is < 0.4V, the chip will be disabled. The compensation capacitor also acts as a soft-start capacitor.
8	8	PHASE	Switch Node. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

Absolute Maximum Ratings (Note 1)

- Control Voltage, V_{CC} ---------- 15V
- BOOT to PHASE, $V_{BOOT-PHASE}$ ---------- 15V
- PHASE to GND
  - DC ---------- –0.5V to 15V
  - < 20ns ---------- –5V to 25V
- UGATE to PHASE
  - DC ---------- –0.3V to ($V_{BOOT-PHASE}$ + 0.3V)
  - < 20ns ---------- –5V to ($V_{BOOT-PHASE}$ + 5V)
- LGATE to GND
  - DC ---------- –0.3V to (V_{CC} + 0.3V)
  - < 20ns ---------- –5V to (V_{CC} + 5V)
- Input/Output Voltage ---------- (GND – 3V) to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 ---------- 0.833W
  - SOP-8 (Exposed Pad) ---------- 1.333/W
- Package Thermal Resistance (Note 2)
  - SOP-8, θ_{JA} ---------- 120°C/W
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Control Voltage, V_{CC} ---------- 4.5V to 13.2V
- Supply Input Voltage, V_{IN} ---------- 2V to 12V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Current	I_{CC}	UGATE, LGATE Open	--	2	--	mA
Shutdown Current	I_{SHDN}	UGATE, LGATE Open	--	1	--	mA
Power On Reset						
Power On Reset Threshold	V_{CCR_TH}	V_{CC} Rising	3.9	4.1	4.3	V
Power On Reset Hysteresis	V_{CC_HYS}		0.26	0.45	0.64	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Frequency	f_{OSC}	RT8116A	250	275	300	kHz
		RT8116B	180	200	220	
Ramp Amplitude	ΔV_{OSC}		--	1.3	--	V_{P-P}
Maximum Duty Cycle			--	85	--	%
Reference						
Reference Voltage	V_{REF}		0.792	0.8	0.808	V
Error Amplifier						
Open Loop DC Gain	A_{DC}	Guaranteed by Design	--	70	--	dB
Gain Bandwidth	GBW	Guaranteed by Design	--	10	--	MHz
Slew Rate	SR	Guaranteed by Design	--	6	--	V/μs
Transconductance	gm		2.8	3.6	--	mA/V
Output Source Current	I_{COMPsr}	$V_{FB} < V_{REF}$	80	120	--	μA
Output Sink Current	I_{COMPsk}	$V_{FB} < V_{REF}$	80	120	--	μA
Input Bias Current			--	0.1	1	μA
Soft Start						
SS Source Current	I_{SS}	$V_{FB} < V_{REF}$	7	10	13	μA
Switch Over Threshold			--	100	--	% of V_{REF}
PWM Controller Gate Driver						
UGATE Drive Source	$I_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 12V, max source current	--	1.2	--	A
UGATE Drive Sink	$R_{UGATEsk}$	$V_{UGATE} - V_{PHASE}$ = 0.1V	--	3	--	Ω
LGATE Drive Source	$I_{LGATEsr}$	V_{CC} = 12V, max source current	--	1.2	--	A
LGATE Drive Sink	$R_{LGATEsk}$	V_{LGATE} = 0.1V	--	1.8	--	Ω
Deadtime between UGATE Off to LGATE On		$V_{UGATE} - V_{PHASE}$ = 1.2V to V_{LGATE} =1.2V	--	30	--	ns
Deadtime Between LGATE Off to UGATE On		$V_{UGATE} - V_{PHASE}$ = 1.2V to V_{LGATE} = 1.2V	--	30	--	ns
Protection						
Under Voltage Protection	V_{UVP_FB}		--	75		%
LGATE OC Setting Current	I_{OCSET}	Sourced from LGATE	9	10	11	μA
Over Current Threshold	V_{PHASE}	R_{OCSET} = Open	--	–375	--	mV
Enable Threshold	V_{EN}		0.3	0.4	0.55	V

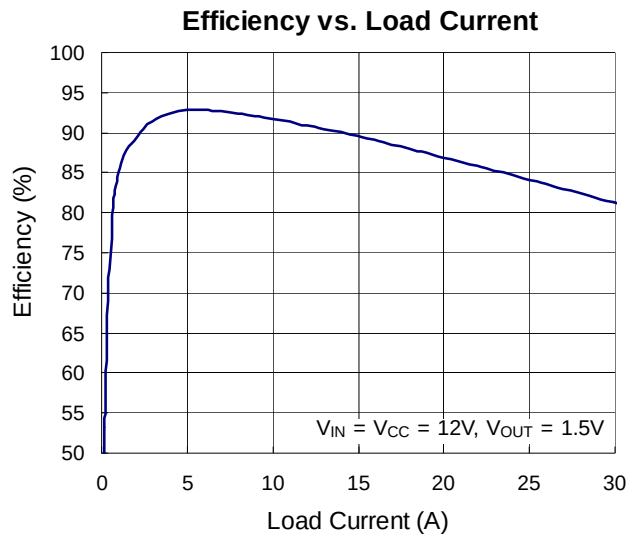
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

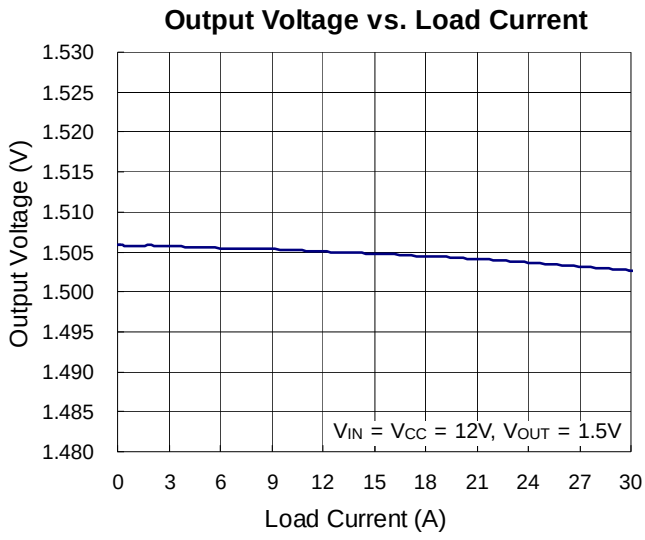
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high-effective four-layer thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The measurement case positions of θ_{JC} are on the lead of the SOP package and on the exposed pad of the PSOP package.

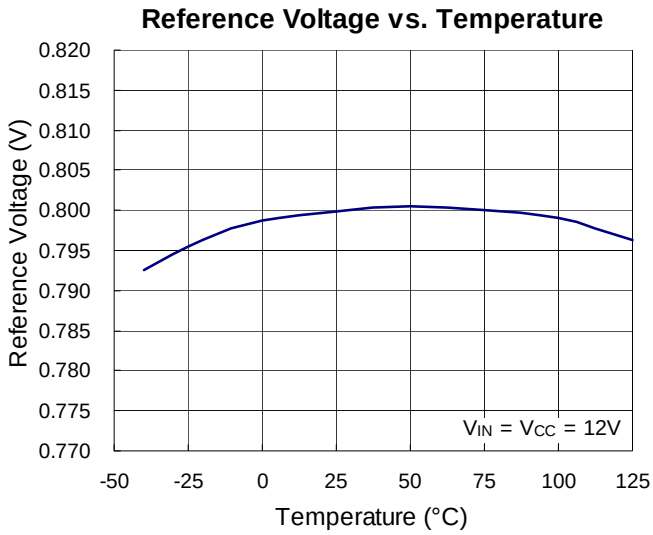
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

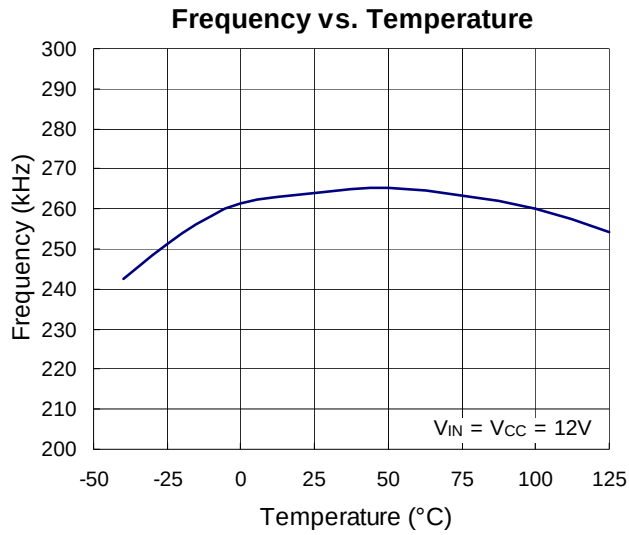
Note 4. The device is not guaranteed to function outside its operating conditions.

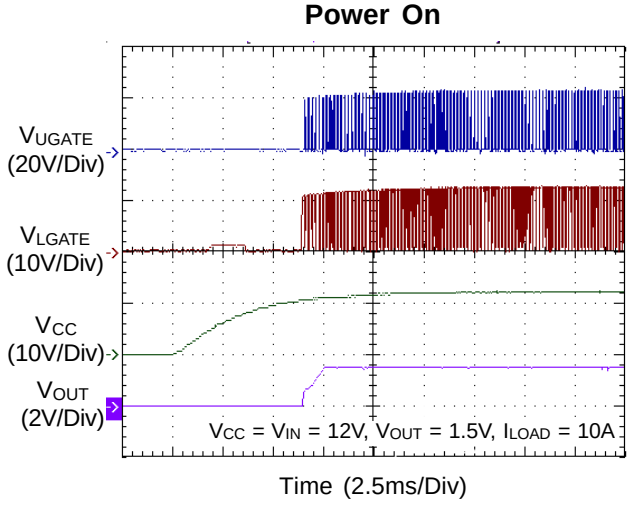
Typical Operating Characteristics

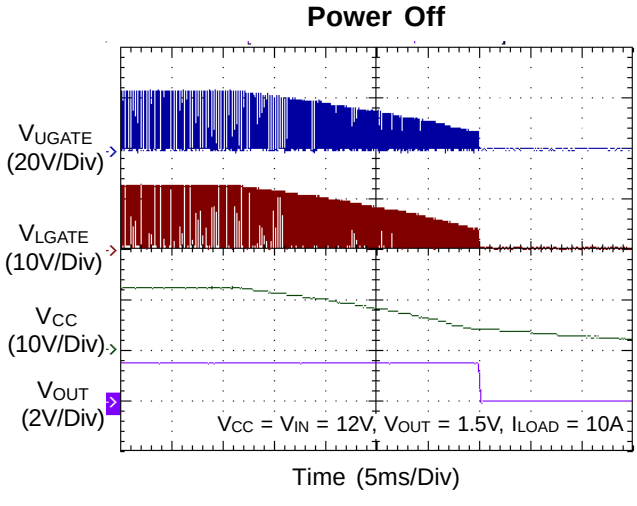




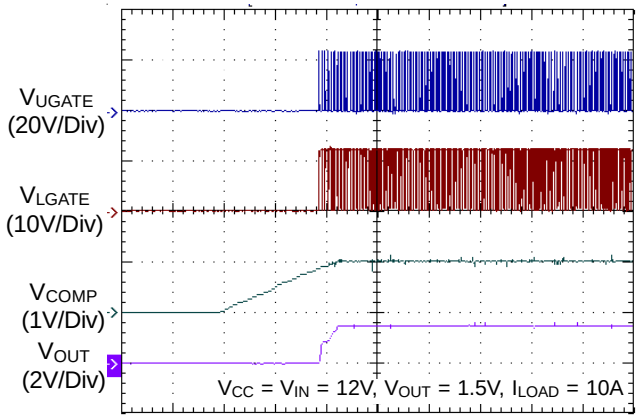




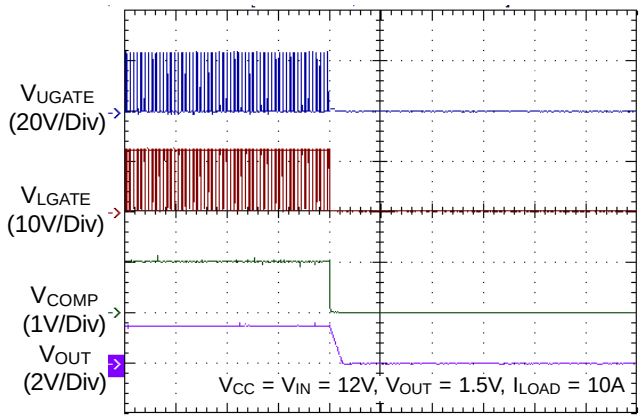




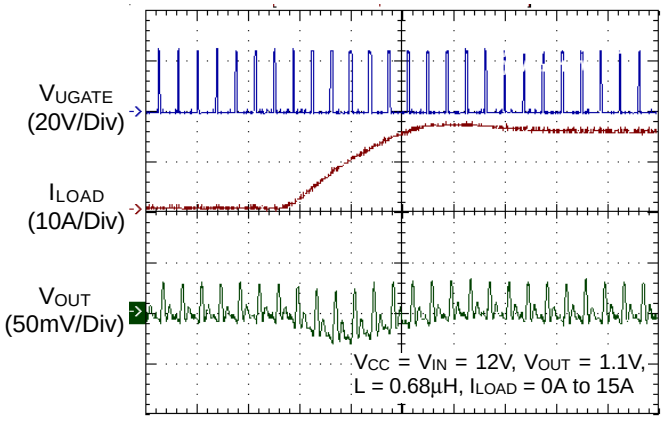
COMP/$\overline{SD}$ Power On



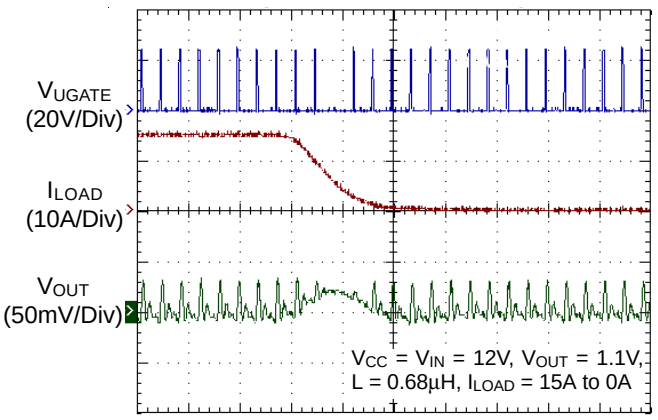
COMP/$\overline{SD}$ Power Off



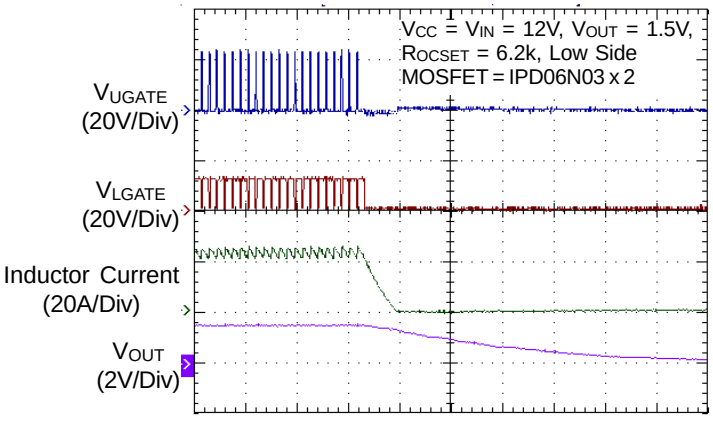
Load Transient Response



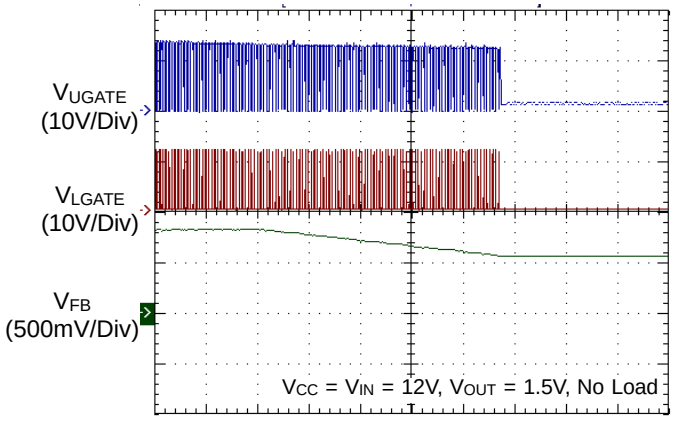
Load Transient Response



Over Current Protection



Under Voltage Protection



Application Information

The RT8116 is a single-phase synchronous buck PWM controller with integrated N-MOSFET gate drivers. It provides single feedback loop, voltage mode control with fast transient response. An internal 0.8V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed frequency oscillator is integrated to eliminate external component count. The RT8116 also provides programmable soft-start function via an external capacitor. Protection features include programmable over current protection and under voltage lockout (UVLO).

Supply Voltage and Power On Reset (POR)

The input voltage range for V_{CC} is from 4.5 V to 13.2 V with respect to GND. An internal linear regulator regulates the supply voltage for internal control logic circuit. A minimum 0.1μF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC.

The V_{CC} powers the integrated MOSFET driver. A bootstrap diode is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications.

The power on reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage (typ. 4V), the controller is reset and prepares the PWM for operation. If VCC falls below the POR falling threshold during normal operation, all MOSFETs stop switching. The POR rising and falling threshold has a hysteresis to prevent noise caused reset.

Chip Enable and Disable

COMP/$\overline{SD}$ pin of RT8116 is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier.

When COMP/$\overline{SD}$ voltage falls or is externally pulled low below the enable level V_{EN}, the chip shuts down. When the controller is shut down, UGATE and LGATE signals will go low. When the pull-down device is released and the COMP/$\overline{SD}$ pin rises above the V_{EN} trip point, the RT8116 will begin a new initialization and soft-start cycle. This allows flexible power sequence control for specified application. In practical applications, connect a small signal MOFSET to COMP/$\overline{SD}$ pin to implement the enable/ disable function.

External Soft-start

The RT8116 provides an external soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. Soft-start begins when the OCP programming is complete. Figure 1 shows the typical soft-start sequence.

During soft-start, an internal current source (10μA) is used to charge the external soft-start capacitor at the COMP/$\overline{SD}$ pin. V_{COMP} rises up, and the PWM Logic and gate drives are enabled. When the feedback voltage crosses 0.8V, the internal 0.8V reference takes over the behavior of the error operational transconductance amplifier and soft-start is complete. The RT8116 turns off the internal 10μA current source when soft-start is complete.

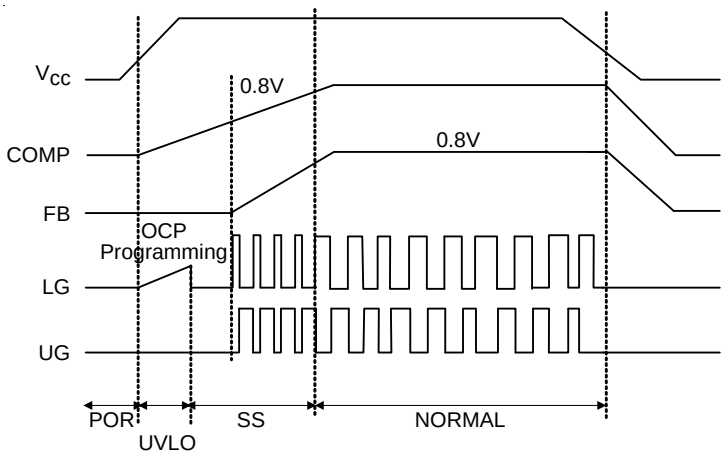


Figure 1. Typical Soft-Start Sequence

Soft-Start Time

To calculate the soft-start time, the following equation can be used.

$$t_{SS} = \frac{(C_P + C_C) \times \Delta V}{I_{SS}}$$

where C_C is the soft-start capacitor and also the compensation capacitor and C_P is the additional capacitor from COMP/$\overline{SD}$ pin to the GND. C_P forms the second pole. I_{SS} is the soft-start current, ΔV is the V_{COMP} voltage from 0.5V to until it reaches regulation.

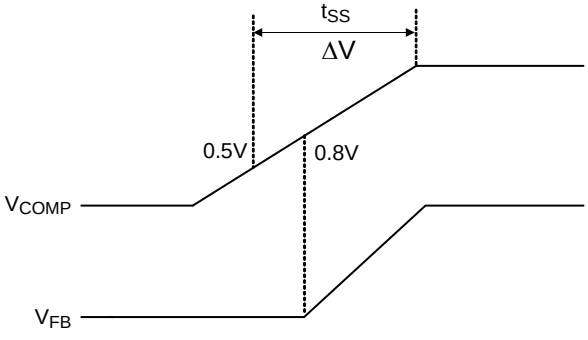


Figure 2. Soft-Start Time

Over Current Protection (OCP)

The RT8116 provides over current protection by detecting the voltage drop across low side MOSFET when it is turned on. The over current trip threshold is programmable by an external resistor at the LGATE pin. When LGATE is turned off, the RT8116 samples and holds the phase voltage. The sample-and-hold voltage represents the inductor current valley and is compared to the OCP threshold. If the sensed phase voltage is lower than the OCP threshold, OCP will be triggered. Both UGATE and LGATE will go low, and the controller will enter the hiccup mode until the OCP condition is released.

LGATE Over Current Setting (LGOCS)

Over current threshold is externally programmed by adding a resistor (R_{OCSET}) between LGATE and GND. Once VCC exceeds the POR threshold, an internal current source I_{OCSET} flows through R_{OCSET}. The voltage across R_{OCSET} is stored as the over current protection threshold V_{OCSET}. After that, the current source is switched off. R_{OCSET} can be determined using the following equation :

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

where I_{VALLEY} represents the desired inductor OCP trip current (inductor current valley), and $R_{LGDS(ON)}$ is the LGATE On-Resistance.

If R_{OCSET} is not present, there will be no current path for I_{OCSET} to build the OCP threshold. In this situation, the OCP threshold is internally preset to 375mV (typical.).

Under Voltage Protection (UVP)

The voltage on the FB pin is monitored for under voltage protection. If the FB voltage is lower than the UVP threshold (typically 75% x VREF) during normal operation, UVP will be triggered. When UVP is triggered, both UGATE and LGATE go low. The controller enters hiccup mode until the UVP condition is removed.

Output Voltage Setting

The RT8116 allows the output voltage of the DC/DC converter to be adjusted from 0.8V to 85% of the V_{IN} supply voltage via an external resistor divider. It will try to maintain the feedback pin at the internal reference voltage.

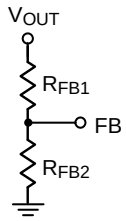


Figure 3. Output Voltage Setting

According to the resistor divider network above, the output voltage is set as :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Input Inrush Current

To calculate the input inrush current, the following equation can be used.

$$I_{INRUSH} = \frac{C_{OUT} \times V_{OUT}}{t_{SS}}$$

where I_{INRUSH} is the input current during start up, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the soft-start time. If the inrush current is higher than the OCP setting current, OCP is triggered.

MOSFET Drivers

The RT8116 integrates high current gate drivers for the MOSFETs to obtain high efficiency power conversion in synchronous buck topology. A dead time is used to prevent

the crossover conduction for high side and low side MOSFETs. Because both the two gate signals are off during the dead time, the inductor current freewheels through the body diode of the low side MOSFET. The freewheeling current and the forward voltage of the body diode contribute to the power loss. The RT8116 employs adaptive dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent cross conduction.

For high output current applications, two or more power MOSFETs are usually paralleled to reduce $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/ sink current capability result in longer rising/ falling time in gate signals, and therefore higher switching loss.

The RT8116 embeds high current gate drivers to obtain high efficiency power conversion. The embedded drivers contribute to the majority of the power dissipation of the controller. Therefore, SOP package is chosen for its power dissipation rating. If no gate resistor is used, the power dissipation of the controller can be approximately calculated using the following equation :

$$P_{DRIVER} = f_{SW} \times (Q_{G\_HIGH\text{-}SIDE} \times V_{BOOT} + Q_{G\_LOW\text{-}SIDE} \times V_{DRIVER\_LOW\text{-}SIDE})$$

where V_{BOOT} represents the voltage across the bootstrap capacitor.

It is important to ensure that the package can dissipate the switching loss and have enough room for safe operation.

Inductor Selection

The inductor plays an important role in step-down converters because it stores the energy from the input power rail and then released the energy to the load. From the viewpoint of efficiency, the DC resistance (DCR) of the inductor should be as small as possible to minimize conduction loss. In addition, because the inductor takes up most of the board space, its size is also important. Low profile inductors can save board space especially when the height has limitation. However, low DCR and low profile inductors are usually cost ineffective.

Larger inductance results in lower ripple current, which means lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade off between performance, size and cost.

In general, the inductance is designed such that the ripple current ranges between 20% to 40% of the full load current. The minimum inductance required can be calculated using the following equation :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_RATED}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between the inductor ripple current and the rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting input capacitors. Conservatively speaking, an input capacitor should have a voltage rating 1.5 times greater than the maximum input voltage to be considered a safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for the RMS current rating. One good design is to use more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank. Placing the ceramic capacitor close to the drain of the high side MOSFET is also helpful in reducing the input voltage ripple during heavy load.

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the buck topology. In steady state condition, the ripple current flowing in and out of the capacitor results in ripple voltage. The output voltage ripples contains two components, ΔV_{OUT_ESR} and ΔV_{OUT_C}.

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times f_{SW}}$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage sag can be

calculated using the following equation :

V_{OUT_SAG} = ESR x ΔI_{OUT}

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore ESL contributes to part of the voltage sag. Use a capacitor that has low ESL to obtain better transient performance. Generally, several capacitors connected in parallel will have better transient performance than just one single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, using a mixed combination of electrolytic capacitor and ceramic capacitor can also achieve better transient performance.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high side MOSFET is small. Therefore, the switching loss of the high side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application.

However, the small duty cycle of the high side MOSFET means that the low side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, the MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on state resistance. However, this depends on the low side MOSFET driver's capability and the budget.

Compensation Network Design

The RT8116 is a voltage mode controller and requires external compensation to have an accurate output voltage regulation with fast transient response.

The RT8116 uses a high gain operational transconductance amplifier (OTA) as the error amplifier. As shown in Figure 4, the OTA works as the voltage controlled current source. The characteristic of OTA is as below :

$gm = \frac{\Delta I_{OUT}}{\Delta V_M}$, where $\Delta V_M = (V_{IN+}) - (V_{IN-})$

and $\Delta V_{COMP} = \Delta I_{OUT} \times Z_{OUT}$

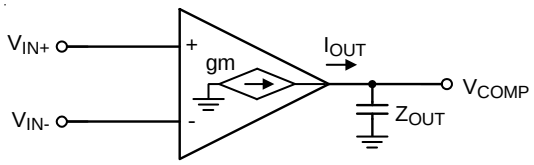


Figure 4. Operational Transconductance Amplifier, OTA

Figure 5 shows a typical buck control loop using Type II compensator. The control loop consists of the power stage, PWM comparator and a compensator. The PWM comparator compares V_{COMP} with the oscillator (OSC) sawtooth wave to provide a pulse width modulated (PWM) with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier.

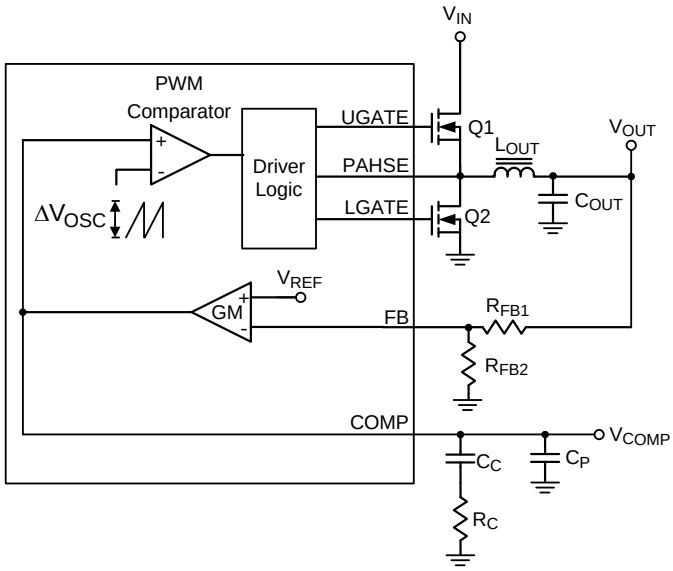


Figure 5. Typical Voltage Mode Buck Converter Control Loop

The modulator transfer function is the small signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output). This transfer function is dominated by a DC gain, a double pole, and an ESR zero as shown in Figure 6.

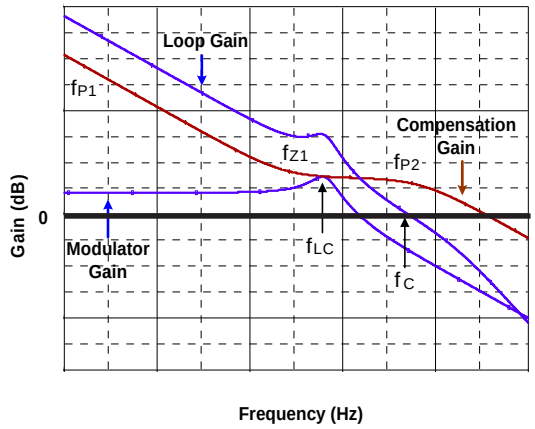


Figure 6. Typical Bode Plot of a Voltage Mode Buck Converter

The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak to peak oscillator voltage, V_{OSC}.

$$Gain_{MODULATOR} = \frac{V_{IN}}{\Delta V_{OSC}}$$

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180°C . The resonant frequency of the LC filter is expressed as :

$$f_{LC} = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor to have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as follows :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The goal of the compensation network is to provide adequate phase margin (usually greater than 45°C) and the highest bandwidth (0dB crossing frequency). It is also recommended to manipulate the loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. According to Figure 5, the compensation network frequency is as below :

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times R_C \times \left(\frac{C_C \times C_p}{C_C + C_P} \right)}$$

$$f_{Z1} = \frac{1}{2\pi \times R_C \times C_C}$$

Determining the 0dB crossing frequency (f_C, control loop bandwidth) is the first step of compensator design. Usually, f_C is set to 0.1 to 0.3 times the switching frequency. The second step is to calculate the open loop modulator gain and find out the gain loss at f_C. The third step is to design a compensator gain that can compensate the modulator gain loss at f_C. The final step is to design f_{Z1} and f_{Z2} to allow the loop to have sufficient phase margin.

f_{Z1} is designed to cancel one of the double poles of the modulator. Usually, place f_{Z1} before f_{LC}. f_{P2} is usually placed below the switching frequency (typically, 0.5 to 1 times the switching frequency) to eliminate high frequency noise.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8116, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 packages, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. For PSOP-8 packages, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for SOP-8 package

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for PSOP-8 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For RT8116 packages, the derating curves in Figure 7 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

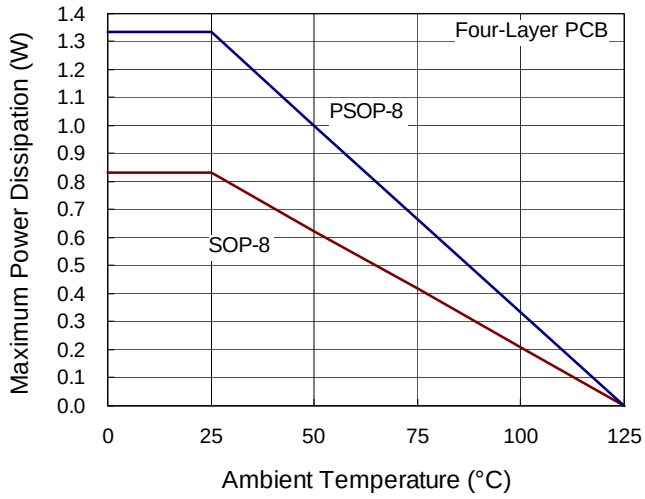


Figure 7. Derating Curves for RT8116 Package

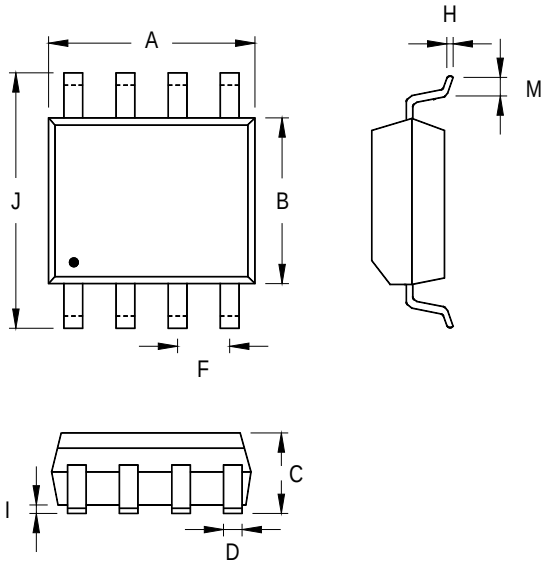
Layout Considerations

Layout planning plays a critical role in modern high frequency switching converter design. A circuit boards with careful layout can help the IC function properly and achieve low losses, low switching noise, and stable operation with improved performance. Without a careful layout, the PCB may radiate excessive noise, causing noise-induced IC problems which contribute to the converter instability. The following guidelines should be strictly followed to have better IC performance.

- Power components should be placed first. Keep the connection between power components as short as possible.
- Input bulk capacitors should be placed close to the drain of the high side MOSFET and the source of the low side MOSFET.
- Place the VCC bypass capacitor as close as possible to the RT8116.
- Minimize the trace length between the power MOSFETs and its drivers.

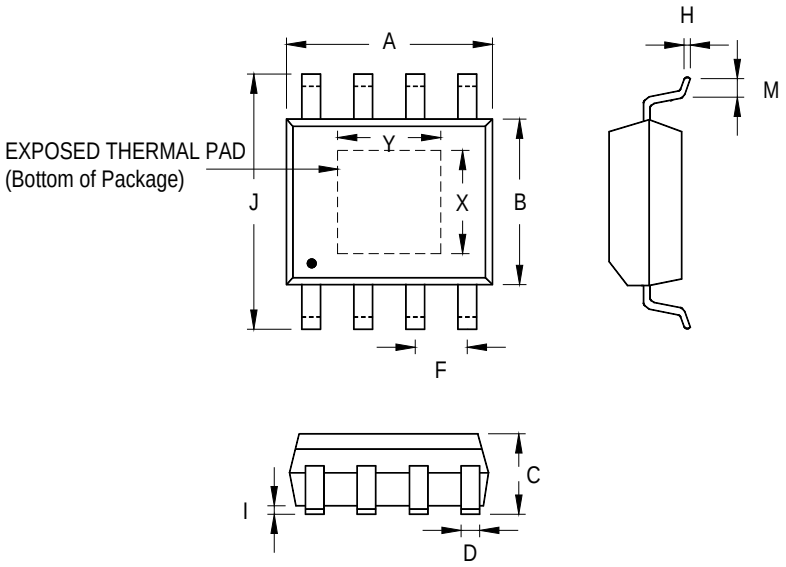
  Since the drivers use short, high current pulses to drive the power MOSFETs, the driving traces should be as short and wide as possible to reduce trace inductance. This is especially true for the low side MOSFET, since this can reduce the possibility of the shoot-through.
- Provide enough copper area around the power MOSFETs and the inductors to aid in heat sinking. Using thick copper PCB can also reduces the resistance and inductance to obtain improve efficiency.
- The bank of the output capacitor should be placed physically close to the load. This can minimize the impedance seen by the load and improve the transient response.
- Place all high frequency decoupling ceramic capacitors close to their decoupling targets.
- Small signal components should be located as close as possible to the IC. Small signal components include feedback components, current sensing components, compensation components, function setting components and any bypass capacitors. These components belong to the high impedance circuit loop and are inherently sensitive to noise pick-up. Therefore, they must be located close to their respective controller pins and away from the noisy switching nodes.
- A multi-layer PCB design is recommended. Make use of one-single layer as the power ground and have a separate control signal ground as the reference of all signals.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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