Wide Input Range Synchronous Buck DC/DC PWM Controller

General Description

The RT8110A is a fixed-frequency PWM controller with integrated MOSFET drivers for single power rail synchronous single-phase buck converter. This part features an internal regulator that allows wide input voltage range operation. The RT8110A utilizes voltage-mode control with internal compensation to simplify the converter design. An internal 0.8V reference voltage allows low output voltage application. The switching frequency is fixed at 600kHz to reduce the external passive component size to save board space. The RT8110A provides under voltage protection, current limit, over current protection and over temperature protection. The low-side MOSFET $R_{DS(ON)}$ is used to sense the inductor current for over current protection.

Ordering Information

RT8110A-□□

Package Type
SP : SOP-8 (Exposed Pad-Option 1)

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

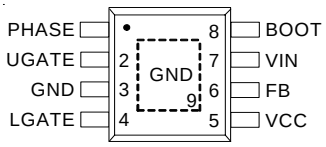
- **10V to 23V Wide Input Voltage Range**
- **0.8V Internal Reference**
- **Internal Soft Start**
- **High DC Gain Voltage Mode PWM Control**
- **Fixed 600kHz Switching Frequency**
- **Fast Transient Response**
- **Fully Dynamic 0 to 80% Duty Cycle**
- **Over Current Protection**
- **Under Voltage Protection**
- **Over Temperature Protection**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Set-top Box Power Supplies
- PC Subsystem Power Supplies
- Cable Modems, DSL Modems
- DSP and Core Communication Processor Power Supplies
- Memory Power Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- Low Voltage Distributed Power Supplies

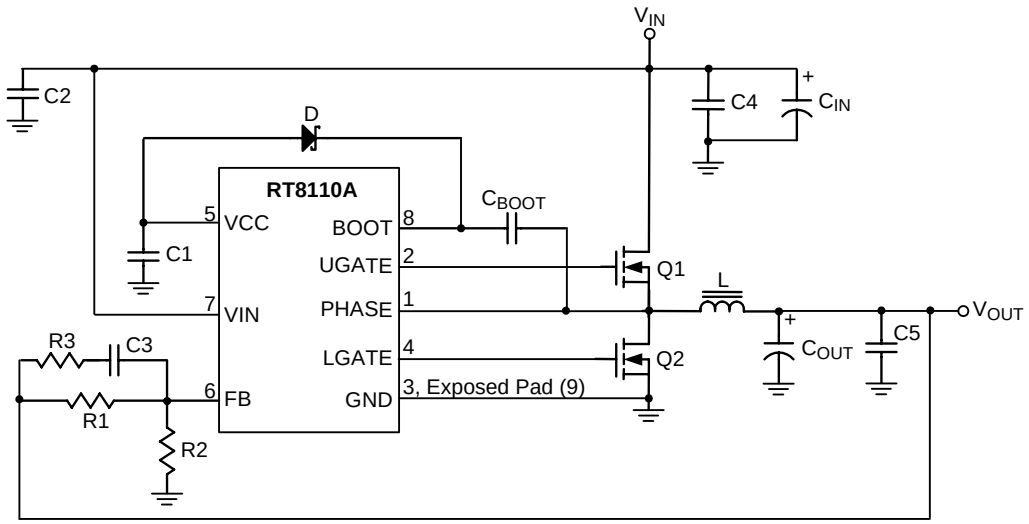
Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

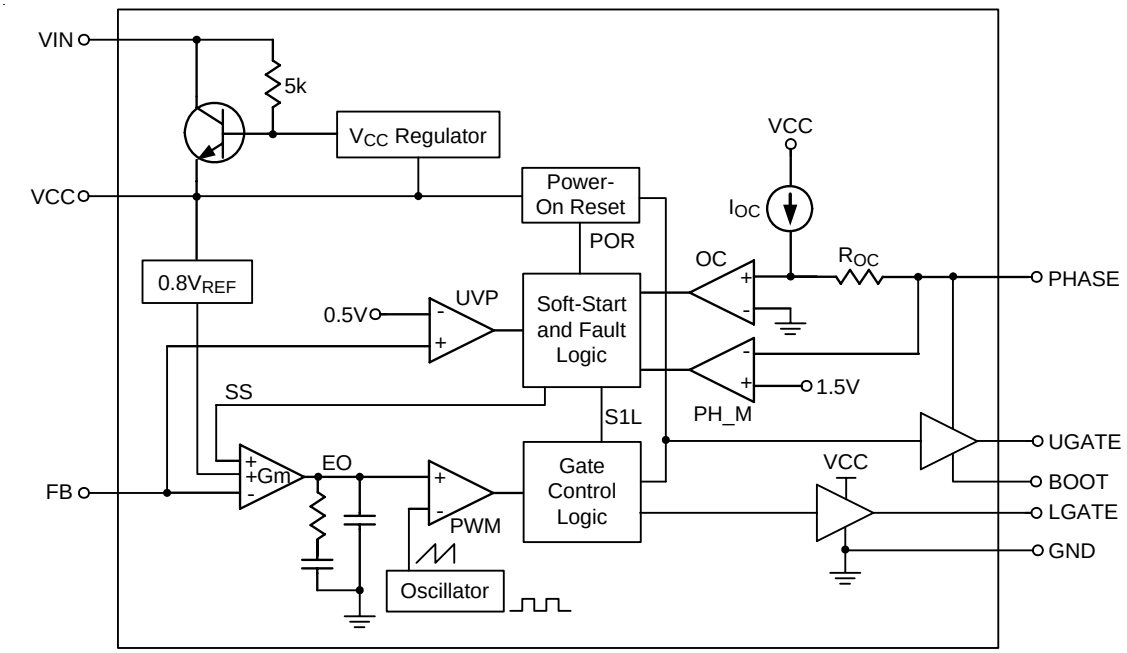
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PHASE	Switching Node of the Buck Converter. This pin is also used to monitor the voltage drop across the low-side MOSFET for over current protection.
2	UGATE	Gate Drive Pin for High-Side MOSFET.
3, 9 (Exposed Pad)	GND	Signal and Power Ground of the IC. All voltage levels are referenced with respect to this pin. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	LGATE	Gate Drive Pin for Low-Side MOSFET.
5	VCC	Internal Regulator Output Pin, typically 5.5V. VIN is regulated to VCC by the internal regulator. VCC is the main bias supply of the IC. This pin also provides power for the low-side MOSFET gate driver. Connect a ceramic capacitor to this pin. The voltage at this pin is monitored for power on reset (POR).
6	FB	Inverting Input of the Error Amplifier. This pin is connected to the joint of output voltage divider resistors to set the output voltage. The voltage at this pin is also monitored for under voltage protection.
7	VIN	This pin is internally connected to the collector of integrated BJT, which is designed to withstand 23V to provide a regulated 5.5V voltage to VCC pin.
8	BOOT	This pin provides power to the high-side MOSFET gate driver. A bootstrap circuit is used to drive the high-side MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 7V
- Supply Voltage, V_{IN} ---------- 30V
- PHASE ---------- –3V to 24V
- BOOT ---------- 30V
- Input/Output Voltage ---------- 0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 10V to 23V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- 0°C to 70°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} Supply Current						
Power Supply Current	I_{CC}	UGATE, LGATE open	--	3	6	mA
Input Voltage Range	V_{IN}		10	--	23	V
Regulated Output Voltage	V_{CC}		--	5.5	--	V
Power-On Reset						
VCC Threshold Voltage		Rising	--	4.7	--	V
VCC Threshold Hysteresis			--	0.9	--	V
Reference						
Reference Voltage	V_{REF}		0.784	0.8	0.816	V
Oscillator						
Free Running Frequency	f_{SW}		480	600	720	kHz
Ramp Amplitude	ΔV_{OSC}		--	2.2	--	V
Error Amplifier						
E/A Transconductance	Gm	Note 5	--	0.3	--	ms
Open Loop DC Gain	A_O	Note 5	60	90	--	dB

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MOSFET Gate Driver						
UGATE Drive Source	$R_{UGATEsr}$	V_{BOOT} – PHASE = 5V V_{BOOT} – V_{UGATE} = 1V	--	3	4.5	Ω
UGATE Drive Sink	$R_{UGATEsk}$	V_{UGATE} –PHASE = 1V V_{BOOT} – PHASE = 5V	--	2	3	Ω
LGATE Drive Source	$R_{LGATEsr}$	V_{CC} – V_{LGATE} = 1V,	--	4	6	Ω
LGATE Drive Sink	$R_{LGATEsk}$	V_{LGATE} = 1V	--	2	4	Ω
UGATE Drive Source	$I_{UGATEsr}$	V_{BOOT} –V_{UGATE} = 5V	--	0.72	--	A
UGATE Drive Sink	$I_{UGATEsk}$	V_{UGATE} –PHASE = 5V	--	0.82	--	A
LGATE Drive Source	$I_{LGATEsr}$	V_{VCC} –V_{LGATE} = 5V	--	0.65	--	A
LGATE Drive Sink	$I_{LGATEsk}$	V_{LGATE} –GND = 5V	--	1.18	--	A
Protection						
Over Current Threshold	V_{OC}	Sense Phase Pin Voltage	––	–250	--	mV
Maximum Duty Cycle			--	80	--	%
UVP Threshold		FB Falling	--	0.5	0.6	V
Soft Start						
Soft Start Interval	T_{SS}		1	3	6	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case position of θ_{JC} is on the exposed pad of the package.

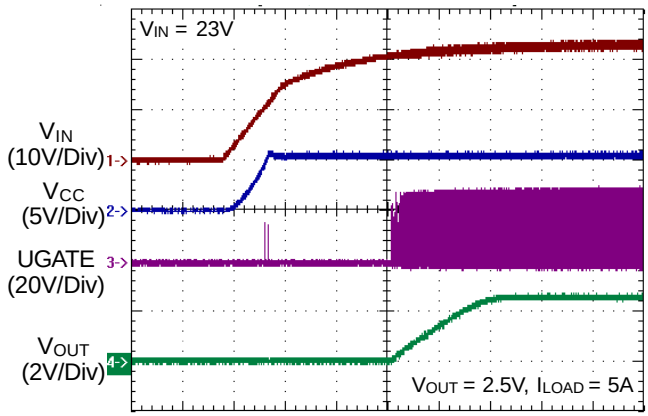
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

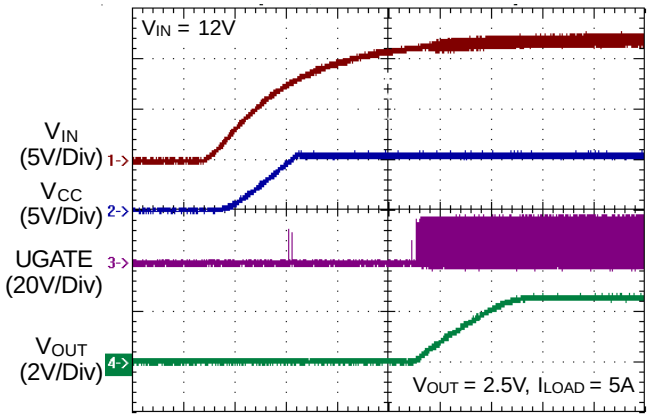
Note 5. Guarantee by design.

Typical Operating Characteristics

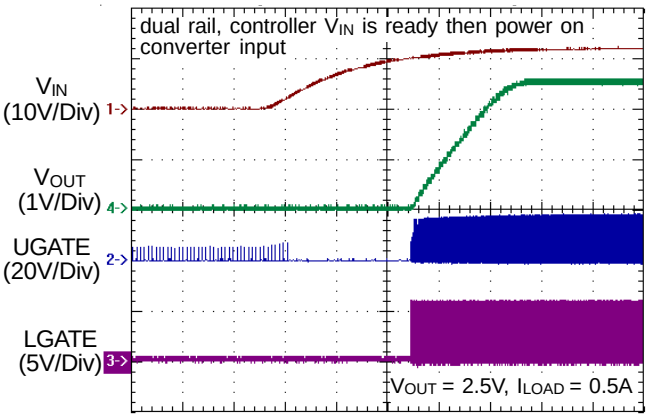
Power On



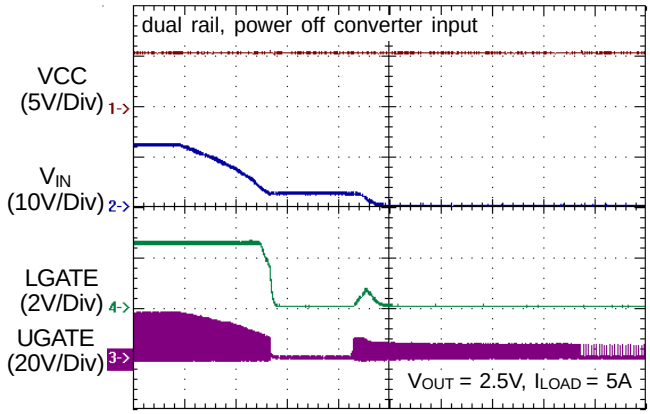
Power On



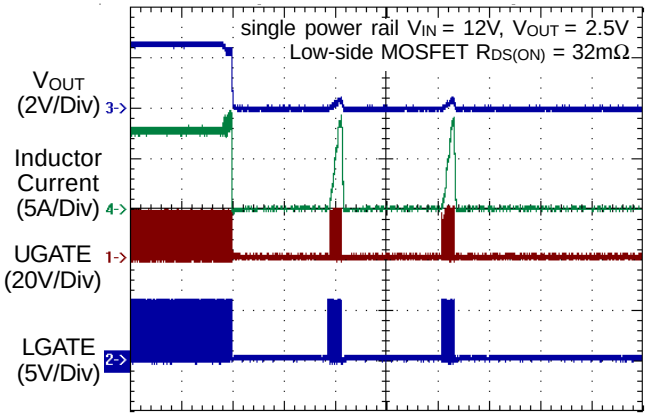
Power On Sequence



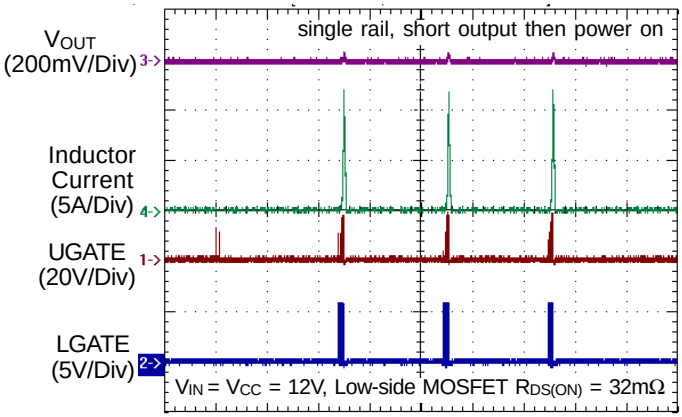
Under Voltage Protection



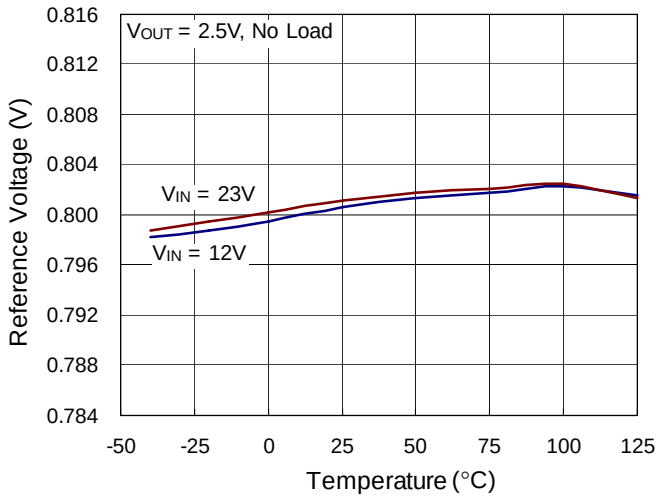
Over Current Protection



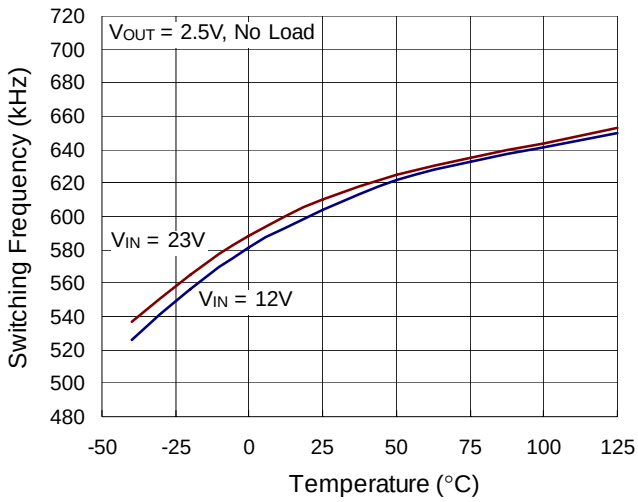
Short Circuit Over Current Protection



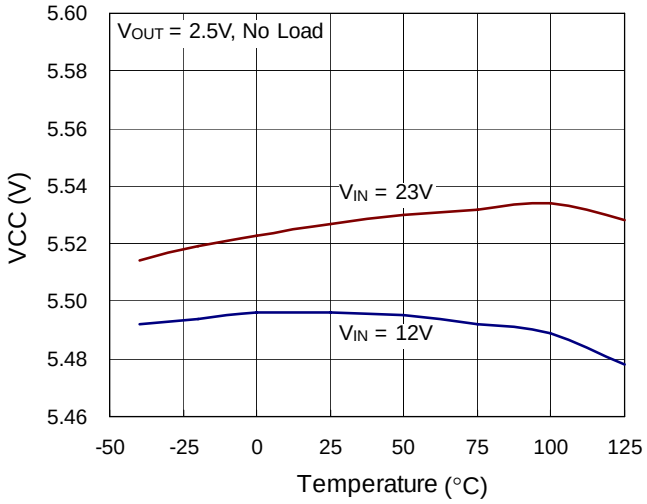
Reference Voltage vs. Temperature



Switching Frequency vs. Temperature



VCC vs. Temperature



Applications Information

The RT8110A is a wide input voltage range, voltage-mode PWM controller with integrated MOSFET gate drivers for single-phase synchronous buck converter. It features an internal regulator, which provides regulated VCC from a wide input range of VIN to power the controller. This part provides internal soft start, internal loop compensation and protection functions.

Internal VCC Regulator

RT8110A can operate with input voltage range from 10V to 23V in single input power applications. The input voltage at VIN pin is internally connected to the integrated bipolar junction transistor and is then regulated to 5.5V by the internal regulator to support VCC. VCC is used as the power of internal control logic circuit and low-side MOSFET gate driver. It is recommended to add a 2.2μF ceramic capacitor to the VCC pin.

Power-up and Soft Start

The power-on-reset (POR) function continuously monitors the voltage at the VCC pin. When VCC rises and exceeds the POR threshold, the controller initiates its power-up sequence with continuous low-frequency, small-width pulses at UGATE (~6kHz). These pulses are used for converter power stage input voltage (V_{IN}) detection. If V_{IN} is applied, the voltage at PHASE pin will rise and fall due to these detection pulses. A digital counter and a comparator are used to record the number of times that voltage at PHASE pin exceeds the internally-defined voltage level (~1.5V). If the voltage at PHASE pin exceeds and below the internally-defined voltage level for two times, detection pulse stops and V_{IN} is recognized to be ready. Once V_{IN} is ready, soft-start will then initiate after a time delay. Otherwise the detection pulse at UGATE continues.

RT8110A provides internal soft start function. Figure 1 shows the PWM comparator and the operational transconductance amplifier (OTA). The OTA has three inputs: reference voltage V_{REF}, feedback voltage signal FB, and soft start signal SS. During the soft start interval, the feedback voltage signal tracks the SS signal. Because SS signal rises from zero in monotone, therefore the PWM duty cycle will increase gradually at start up to prevent large inrush current. When FB voltage reaches V_{REF}, soft start ends and FB will track V_{REF}. The typical soft start time interval is 3ms

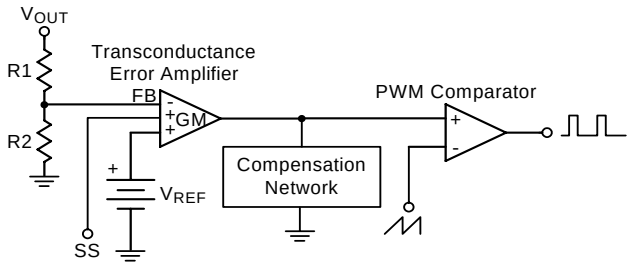


Figure 1. Transconductance Amplifier and PWM Comparator.

Bootstrap Circuit

Figure 2 shows the bootstrap gate drive circuit supplied from VCC. The bootstrap circuit consists of bootstrap capacitor C_{BOOT} and blocking diode D_{BOOT}. The selection of these two components can be done after choosing the high-side MOSFET. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. The capacitance is determined using the following equation :

$$C_{BOOT} = \frac{Q_{GATE}}{\Delta V_{BOOTSTRAP}}$$

where Q_{GATE} is the total gate charge of the high-side MOSFET, and $\Delta V_{BOOTSTRAP}$ is the voltage drop allowed on the high-side MOSFET gate drive. For example, the total gate charge for MOSFET is about 30nC. For an allowed voltage drop of 300mV, the required bootstrap capacitance is 0.1μF.

Referring to Figure 2, the bootstrap diode must be able to block the power stage supply voltage plus any peak ringing voltage at the PHASE pin when Q1 is turned on. Therefore, the voltage rating of the bootstrap diode should be at least 1.5 to twice of the power stage supply voltage.

Since the $R_{DS(ON)}$ of MOSFET will be higher if the gate-to-source driving voltage is lower, a bootstrap diode with larger forward voltage results in lower gate drive voltage, higher on-resistance and lower efficiency. Therefore, the forward voltage of the bootstrap diode should be low. Fast recovery diode or Schottky diode which has low forward voltage is recommended for the bootstrap diode.

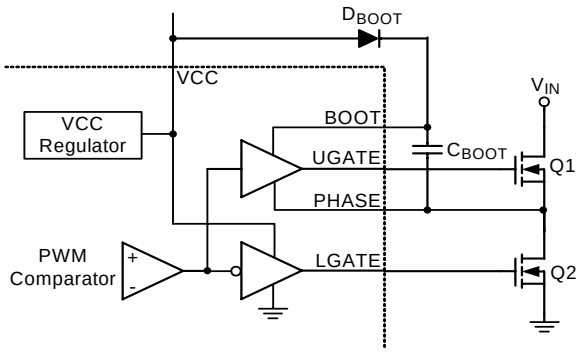


Figure 2. Gate Driver and Bootstrap Circuit

Current Limit and Over Current Protection (OCP)

RT8110A provides current limit and over current protection. The low-side MOSFET on-resistance is used to sense the inductor current. Once the high-side MOSFET is turned off, the low-side MOSFET is turned on when dead time ends. Inductor current then flows through the low-side MOSFET and build a voltage drop across the drain and source (PHASE to GND). This voltage is sensed to monitor the inductor peak current.

As shown in Figure 3, the over current threshold is determined internally by the current source I_{OC} and the internal resistor R_{OC}. The current source I_{OC} flows through resistor R_{OC} and builds voltage V_{OC} ($=I_{OC} \times R_{OC}$) which is referenced to the PHASE pin. When load current increase and the sensed PHASE voltage falls below V_{OC} in one switching cycle, controller will treat this as an over current event. Each over current event will cause one UGATE PWM pulse to be prohibited, but has no influence on LGATE signal, it still keep switching. UGATE PWM pulse is permitted when over current event does not exist. If over current event does not occur in the next switching cycle, UGATE will switch again, or the UGATE pulse will still be prohibited. In this way, inductor peak current will be limited.

If the load current further increases, either over current protection or under voltage protection will be tripped. The over current protection will be tripped when the over current event occurs for continuously four PWM pulses. When OCP is triggered, both UGATE and LGATE go low, controller will initiate re-start in hiccup way. For OCP, controller has three times of hiccupped re-start before shutdown. Controller will latch off after three times of hiccup.

The OCP threshold is determined by the $R_{DS(ON)}$ of low-side MOSFET. The inductor peak current I_{PEAK} can be calculated using the following equation.

$$I_{PEAK} \cong \frac{V_{OC}}{R_{DS(ON)}}$$

Note that I_{PEAK} is the inductor peak current, therefore, I_{PEAK} should be set to be greater than $I_{OUT(MAX)} + (\Delta I)/2$ to prevent false tripping, where ΔI is the output inductor ripple current, and $I_{OUT(MAX)}$ is the maximum load current. Since MOSFET $R_{DS(ON)}$ increases with temperature, the controller will trip OCP/current limit earlier at high temperature. To avoid false tripping, considering the highest junction temperature of the MOSFET and calculate the OCP threshold to select $R_{DS(ON)}$.

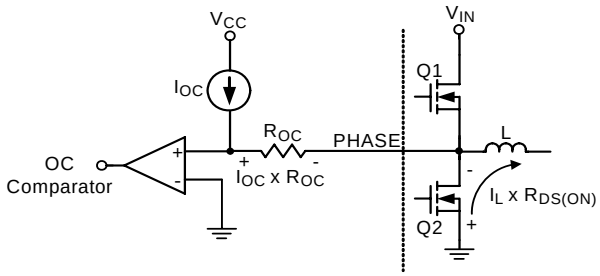


Figure 3. Over Current Protection Mechanism

Under Voltage Protection (UVP)

After soft start completes, the FB voltage is monitored for UVP. The UVP function has a 10µs delay time and the threshold is typically 0.5V. If FB voltage falls below the threshold, UVP will be tripped, both UGATE and LGATE go low and then the hiccupped re-start will be initialized. The UVP re-start behavior is different from that of OCP; the controller will always initiate re-start in a hiccupped way.

Over Temperature Protection (OTP)

The RT8110A integrates thermal protection function. The over temperature protection is a latched protection and its threshold is typically 160°C. When OTP is triggered, controller shuts down, both high-side and the low-side MOSFET are turned off.

Input Capacitor Selection

The input capacitor not only reduces the noise and voltage ripple on the input, but it also reduces the peak current drawn from the power source. The input capacitor must meet the RMS current requirement imposed by the switching current defined by the following equation:

$$I_{RMS} = \frac{I_{OUT} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

The input RMS current varies with load and input voltage, and has a maximum of half the output current when output voltage is equal to half the input voltage. In addition, ceramic capacitor is recommended for high frequency decoupling because of its low equivalent series resistance and low equivalent inductance. These ceramic capacitors should be placed physically between and close to the drain of high-side MOSFET and the source of the low-side MOSFET.

The voltage rating is another key parameter for the input capacitor. In general, choose the voltage rating with 50% higher than the input voltage for the input capacitor to ensure the operation reliability.

Output Voltage Setting

The converter output voltage can be set by the external voltage divider resistors. Figure 4 shows the connection of the output voltage divider resistors. The controller will regulate the output voltage according to the ratio of the voltage divider resistors R1 and R2.

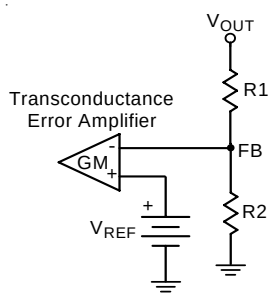


Figure 4. Voltage Divider Resistors

If R1 is given and the output voltage is specified, then R2 can be determined using the following equation :

$$R2 = R1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right)$$

Feedback Compensation and Output Capacitor Selection

The RT8110A is a voltage-mode PWM controller, it uses operational transconductance amplifier (OTA) with internal compensation network to eliminate external compensation components.

The compensation network is used to shape the gain curve to obtain accurate dc regulation, fast load transient response and maintain stability. Figure 5 shows the Bode plot of the modulation gain, compensation gain and the close loop gain. A stable control loop has a close gain curve with a -20dB/decade slope at the crossover frequency and the phase margin is greater than 45°.

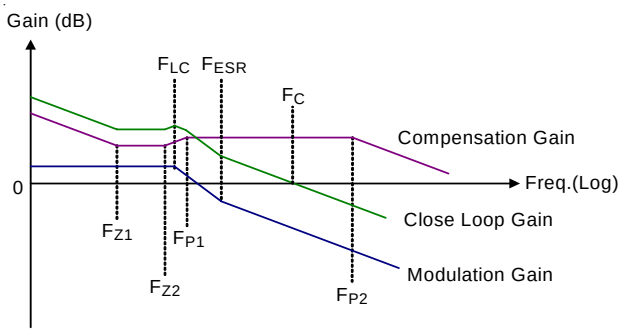


Figure 5. Bode Plot of Loop Gain.

Figure 6 illustrates the simplified synchronous buck converter using OTA with internal compensation. The feedback loop consists of Zin (R1, R2 and C1), OTA and the internal compensation network Z_{FB} (R_S, C_S, C_P). The value of internal compensation component is : $R_S \approx 50k$, $C_S \approx 4nF$, $C_P \approx 10pF$.

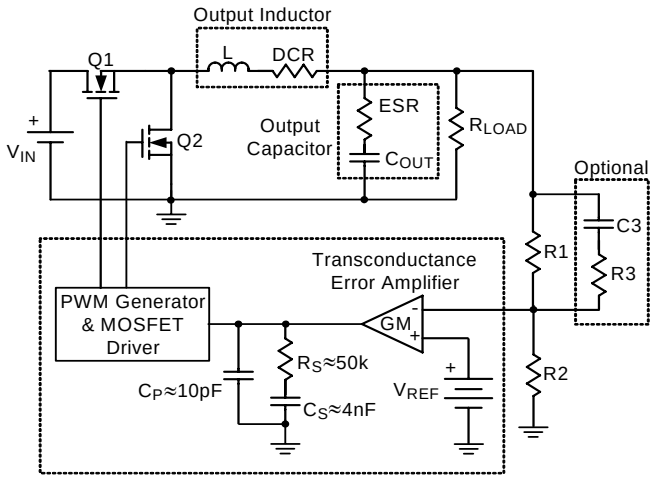


Figure 6. Simplified Diagram for Synchronous Buck Converter with Internal Compensation Network

Referring to Figure 5, the location of pole and zero of the LC filter and the compensation network can be determined using the following equations. The inductor and the output capacitor create a double pole at F_{LC} :

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

The equivalent series resistance (ESR) of the output capacitor creates a zero at F_{ESR} :

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The internal compensation network introduces a zero at F_{Z1} :

$$F_{Z1} = \frac{1}{2\pi \times R_S \times C_S}$$

The internal compensation network also introduces a pole at F_{P2} :

$$F_{P2} = \frac{1}{2\pi \times R_S \times \left(\frac{C_S \times C_P}{C_S + C_P}\right)}$$

The external R3 and C3 introduces a zero at F_{Z2} :

$$F_{Z2} = \frac{1}{2\pi \times (R3 + R2) \times C3}$$

The external R3 and C3 introduces a pole at F_{P1} :

$$F_{P1} = \frac{1}{2\pi \times (R3 + R1 \,//\, R2) \times C3}$$

Since the internal compensation values are given, the close loop crossover frequency and phase margin can be obtained after inductance and capacitance are determined. External R3 and C3 are used to adjust the crossover frequency and phase margin. The typical design procedure is described as follows.

Step 1 : Collect system parameters such as switching frequency, input voltage, output voltage, output voltage ripple, and full load current.

Step 2 : Determine the output inductance value. The recommended inductor ripple current is between 10% and 30% of the full load output current. The inductance can be calculated using the following equation.

$$\frac{V_{IN} - V_{OUT}}{I_{FULL\_LOAD} \times 0.3} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}} < L$$

$$< \frac{V_{IN} - V_{OUT}}{I_{FULL\_LOAD} \times 0.1} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}$$

Step 3 : Determine the output capacitance and the ESR. Neglecting the equivalent series inductance of the output capacitor, the output capacitance C_{OUT} can be approximately determined using the following equations.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = I_{RIPPLE} \times ESR$$

$$V_{RIPPLE(C)} = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}$$

Step 4 : Calculate the crossover frequency, phase margin and check stability.

Calculate the frequency of F_{LC}, F_{ESR}, F_{Z1}, F_{Z2}, F_{P1} and F_{P2} with selected inductance, capacitance and ESR. Then plot the Bode diagram of close loop gain to check crossover frequency and phase margin. In general, the crossover frequency F_C is between 1/10 and 1/5 of the switching frequency (60kHz to 120kHz); and the phase margin should be greater than 45°.

If the bandwidth and phase margin are not within an acceptable range, add R3 and C3 to slightly adjust the crossover frequency and phase margin.

If the crossover frequency and phase margin still can't meet the requirement after tuning R3 and C3, re-select the ESR and C_{OUT} (mainly) or inductance value to change the location of F_{LC} and F_{ESR} then repeat step 4. Note that the output voltage ripple and transient response should still meet the specification after changing ESR, C_{OUT} or L.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of

RT8110A, The maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 (exposed pad) packages, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C - 25°C) / (75°C/W) = 1.333W for

SOP-8 (exposed pad)

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8110A package, the Figure 7 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

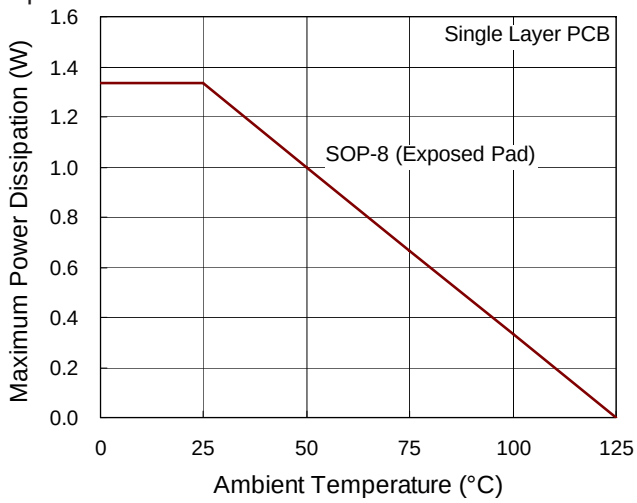


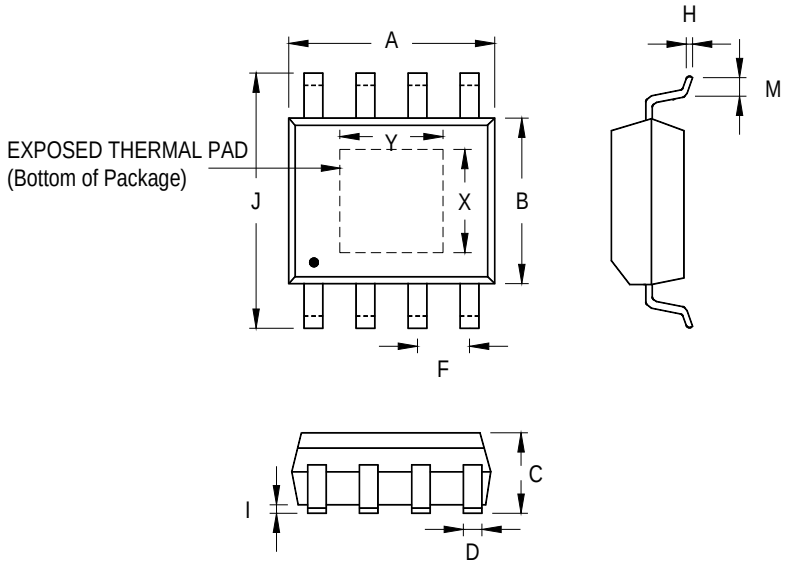
Figure 7. Derating Curves for RT8110 Package

Layout Guidelines

PCB layout plays an important role for RT8110A since its switching frequency is 600kHz. PCB with carefully layout can help to decrease switching noise for stable operation and better performance. The following guidelines can be used in PCB layout.

- Feedback voltage divider resistors, compensation RCs, bootstrap capacitor, bootstrap diode and ceramic capacitors for VIN and VCC should be placed close to the controller as possible.
- Keep the power loops as short as possible. The current transition from one device to another at high speed causes voltage spikes due to the parasitic components on the circuit board. Therefore, all the current switching loops should be kept as short as possible with wide traces to minimize the parasitic components.
- Minimize the trace length between the MOSFET and the controller. Since the drivers are integrated in the controller, the driving path should be short and wide to reduce the parasitic inductance and resistance.
- Place the ceramic capacitor physically close to the drain of the high-side FET and source of low-side FET. This can reduce the input voltage ringing at heavy load.
- Place the output capacitor physically close to the load. This can minimize the impedance seen by the load, and then improves the transient response.
- The voltage feedback trace should be kept away from the switching node. Keep the voltage feedback trace away from the PHASE node, inductor and MOSFETs due to, these switching node/ components are noisy.

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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