

## 1A 1.5MHz 6V Synchronous Buck Converter

### DESCRIPTION

The BL8025 is a high-efficiency, DC-to-DC step-down switching regulators, capable of delivering up to 1A of output current. The device operates from an input voltage range of 2.6V to 6.0V and provides an output voltage from 0.6V to  $V_{IN}$ , making the BL8025 ideal for low voltage power conversions. Running at a fixed frequency of 1.5MHz allows the use of small external components, such as ceramic input and output caps, as well as small inductors, while still providing low output ripples. This low noise output along with its excellent efficiency achieved by the internal synchronous rectifier, making BL8025 an ideal green replacement for large power consuming linear regulators. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

BL8025 is housed in a SOT23-5 Package

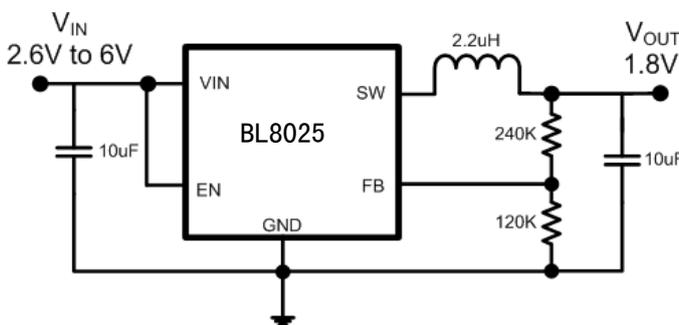
### FEATURES

- High Efficiency: Up to 96%
- Capable of Delivering 1A ( $V_{IN} \geq 3.3V$ )
- 1.5MHz Switching Frequency
- No External Schottky Diode Needed
- Low dropout 100% Duty operation
- Internal Compensation and Soft-Start
- Current Mode control
- 0.6V Reference for Low Output voltages
- Logic Control Shutdown ( $I_q < 1\mu A$ )
- Thermal shutdown and UVLO
- Available in SOT23-5

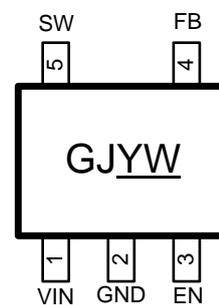
### APPLICATIONS

- Cellular phones
- Digital Cameras
- MP3 and MP4 players
- Set top boxes
- Wireless and DSL Modems
- USB supplied Devices in Notebooks
- Portable Devices

### TYPICAL APPLICATION



### PIN OUT & MARKING



SOT23-5

GJ: Product Code

YW: Date code (Year & Week)

## ORDERING INFORMATION

PART No.	PACKAGE	Tape&Reel
BL8025CB5TR	SOT23-5	3000/Reel

## ABSOLUTE MAXIMUM RATING

Parameter	Value
Max Input Voltage	6.3V
Max Operating Junction Temperature(Tj)	125°C
Ambient Temperature(Ta)	-40°C – 85°C
Maximum Power Dissipation	SOT23-5 400mW
Storage Temperature(Ts)	-40°C - 150°C
Lead Temperature & Time	260°C, 10S
ESD (HBM)	>2000V

Note: Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.

## RECOMMENDED WORK CONDITIONS

Parameter	Value
Input Voltage Range	Max. 6V
Operating Junction Temperature(Tj)	-20°C –125°C

## ELECTRICAL CHARACTERISTICS

(VDD=5V, TA=25°C)

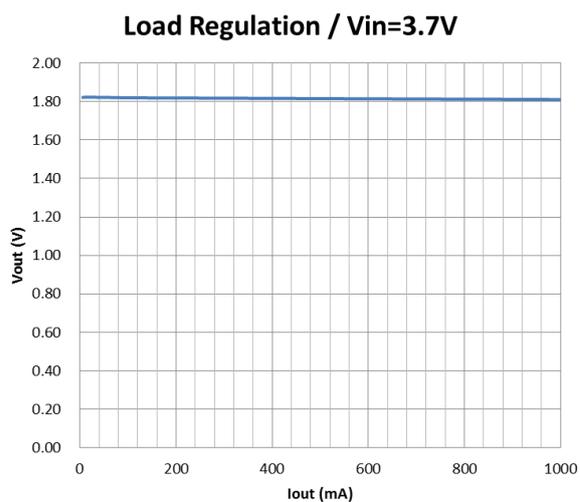
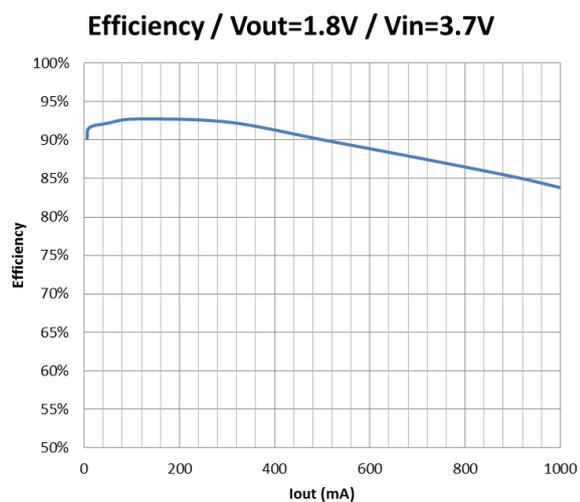
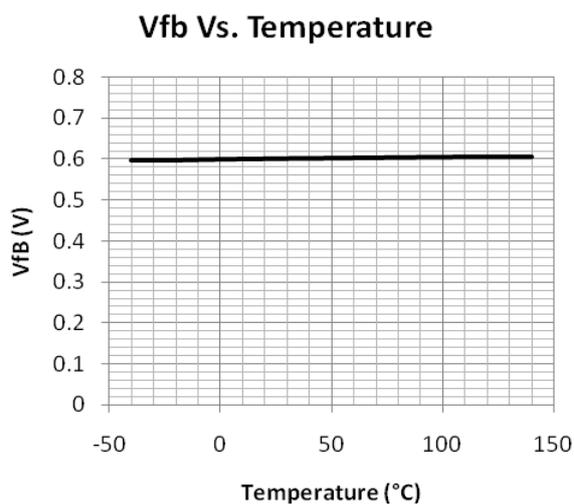
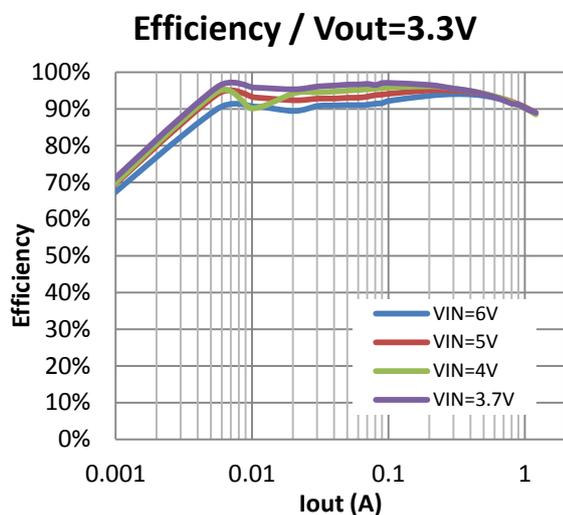
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Input Voltage Range		2.6		6.0	V
Vref	Feedback Voltage	Vin=5V	0.585	0.6	0.615	V
I <sub>fb</sub>	Feedback Leakage current			0.1	0.4	uA
I <sub>q</sub>	Quiescent Current	Active, V <sub>fb</sub> =0.65, No Switching		40		uA
		Shutdown			1	uA
LnReg	Line Regulation	Vin=2.7V to 5.5V		0.04	0.2	%/V
LdReg	Load Regulation	I <sub>out</sub> =0.01 to 1A		0.1	0.2	%/A
F <sub>soc</sub>	Switching Frequency		1.3	1.5	1.7	MHz
R <sub>dsonP</sub>	PMOS R <sub>dson</sub>			280	350	mohm
R <sub>dsonN</sub>	NMOS R <sub>dson</sub>			190	250	mohm
I <sub>limit</sub>	Peak Current Limit	Vin ≥ 3.3V	1.2	1.5	2	A
I <sub>swlk</sub>	SW Leakage Current	V <sub>out</sub> =5.5V, V <sub>SW</sub> =0 or 5.5V, EN=0V			10	uA
I <sub>enlk</sub>	EN Leakage Current				1	uA
V <sub>h_en</sub>	EN Input High Voltage		1.5			V
V <sub>l_en</sub>	EN Input Low Voltage				0.4	V

## PIN DESCRIPTION

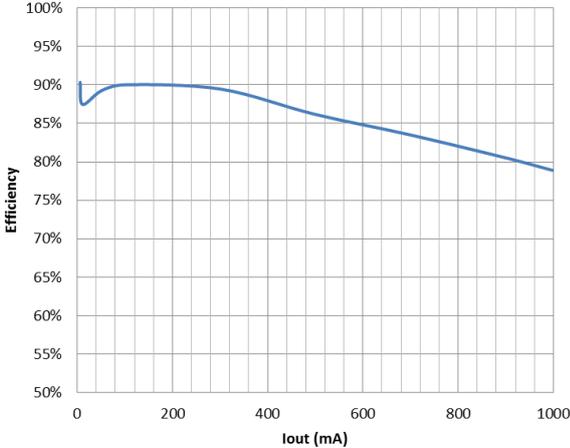
PIN #	NAME	DESCRIPTION
1	VIN	Supply voltage.
2	GND	Ground
3	EN	Enable pin for the IC. Drive the pin to high to enable the part, and low to disable
4	FB	Feedback input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and Vin
5	SW	Inductor connection. Connect an inductor between SW and the regulator output.

## ELECTRICAL PERFORMANCE

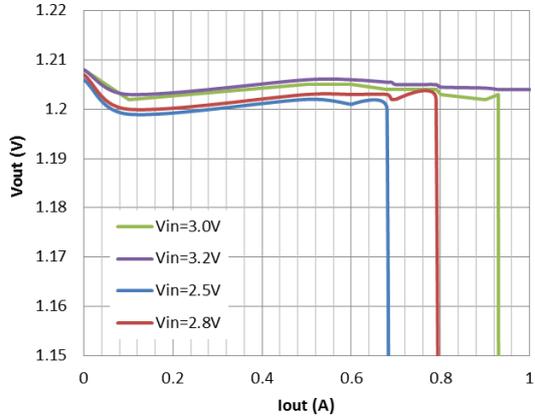
Tested under  $T_A=25^{\circ}\text{C}$ , unless otherwise specified



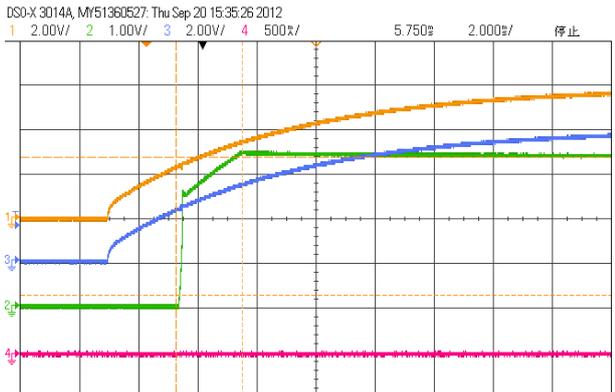
### Efficiency / Vout=1.2V / Vin=3.7V



### Load Capability at Low Vin Vout=1.2V

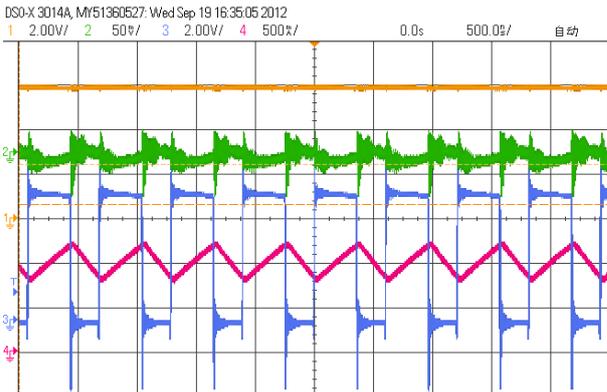


### Power up



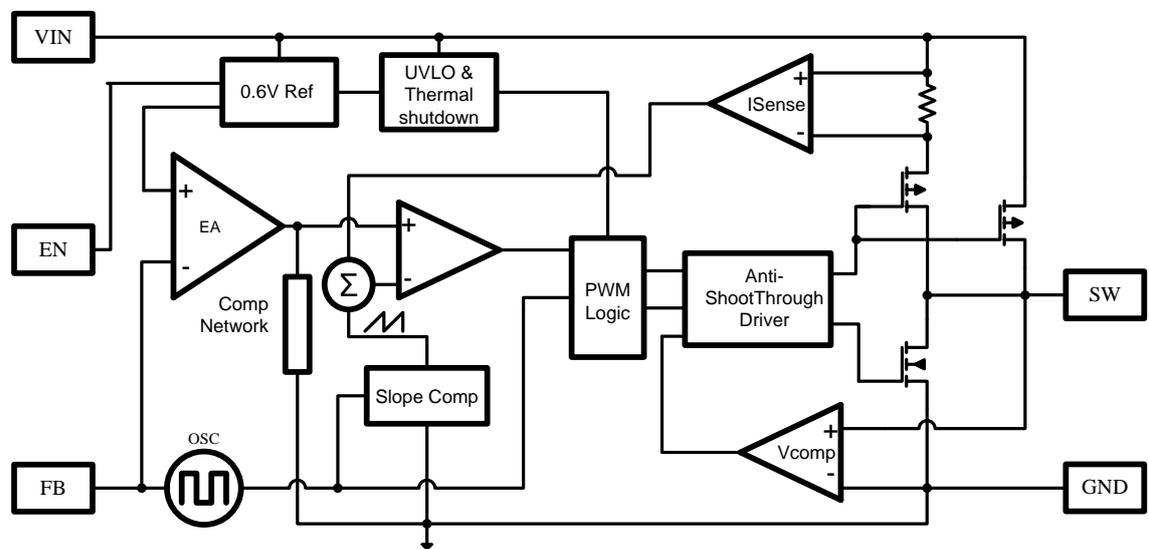
Ch1: Vin, Ch2: Vout, Ch3 EN

### Output Ripple and SW at 1A load Vin=6V / Vout=3.3V



Ch1: Vin, Ch2: Vout, Ch3 SW, Ch4: I\_inductor

## BLOCK DIAGRAM



## DETAILED DESCRIPTION

The BL8025 high-efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 1A of output current. The device operates in pulse-width modulation (PWM) at 1.5MHz from a 2.6V to 5.5V input voltage and provides an output voltage from 0.6V to VIN, making the BL8025 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

### **Loop Operation**

BL8025 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

### **Current Sense**

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

### **Current Limit**

There is a cycle-by-cycle current limit on the high-side MOSFET of 1.5A(typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier

turns on. BL8025 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to 1.5A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

### **Soft-start**

BL8025 has a internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the I soft-start circuitry slowly ramps up current available at SW.

### **UVLO and Thermal Shutdown**

If VIN drops below 2.5V, the UVLO circuit inhibits switching. Once VIN rises above 2.6V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

## Design Procedure

### **Setting Output Voltages**

Output voltages are set by external resistors. The FB\_threshold is 0.6V.

$$RTOP = RBOTTOM[(VOUT / 0.6) - 1]$$

### **Input Capacitor Selection**

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input

source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic

exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$$VRIPPLE = IL(PEAK)[1 / (2\pi \times f_{OSC} \times C_{OUT})]$$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:  
 $VRIPPLE(ESR) = IL(PEAK) \times ESR$

## Application Information

Layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

- 1) Place decoupling capacitors as close to the IC as possible
- 2) Connect input and output capacitors to the same power ground node with a star ground configuration then to IC ground.
- 3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (C1 to VIN and C1 to GND) short. Avoid vias in the switching paths.
- 4) If possible, connect VIN, SW, and GND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
- 5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
- 6) Route high-speed switching nodes away from sensitive analog areas

## PACKAGE OUTLINE

Package	SOT23-5	Devices per reel	3000	Unit	mm
Package specification:					
<p>The drawing shows the mechanical specifications for the SOT23-5 package. The top view shows a total width of 2.9±0.2 mm and a distance of 1.9±0.2 mm between the two top pins (labeled 5 and 4). The distance between the two bottom pins (labeled 1, 2, and 3) is 0.4±0.1 mm. The total height of the package is 2.8±0.3 mm, with a distance of 1.6±0.1 mm from the top edge to the bottom pins. The side view shows a maximum height of 1.1<sup>+0.2</sup>/<sub>-0.1</sub> mm and a distance of 0.8±0.1 mm from the top edge to the top of the package body. The bottom view shows a distance of 0.15<sup>+0.1</sup>/<sub>-0.05</sub> mm from the bottom edge to the bottom of the package body, with a minimum thickness of 0.2 mm. A gap of 0 to 0.1 mm is shown between the package body and the bottom pins.</p>					